Modeling, System Identification, and Control of Interleaved DC-DC Converters

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STATUTORY DECLARATION

I hereby declare that the thesis submitted is my own unaided work, that I have not used other than the sources indicated, and that all direct and indirect sources are acknowledged as references.

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Linz, March 2019

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ABSTRACT

The increasing amount of required functionality in today’s electronic devices demands for more advanced power supply concepts. A possible solution to increase the performance and efficiency of DC-DC converters is to use multi-phase topologies. These converters employ multiple parallel power stages, hence sharing the total load current. In order to provide a regulated output voltage and equal sharing of the total current, a control concept is an essential part of such a converter. Furthermore, the importance of online system identification (SI) in power electronics is ever increasing. It enables the tracking of variable system parameters, which in turn can be used for online controller tuning.

This thesis presents a novel digital constant frequency sliding mode control (SMC) law for interleaved multi-phase DC-DC converters. Both constant switching frequency and interleaving are achieved by dynamically adjusting the hysteresis band of the comparators that generate the control signals. The proposed interleaving method neither imposes constraints on the number of required phases to obtain a specific output voltage nor uses a quasi-SMC law as other implementations for interleaved converters typically do. The suggested control concept accomplishes an accurate output voltage regulation and an improved dynamic performance in comparison with quasi-SMC.

In order to detect the employed converter configuration, a state-space-based SI approach utilizing the step-adaptive approximate least squares estimation algorithm is proposed. The presented approach accurately provides the parameters of the converter’s state-space model while simultaneously featuring a fast convergence rate and low computational complexity. In comparison with state-of-the-art parametric SI methods, the number of required multiplications is more than halved, while accuracy is improved. Consequently, the estimated converter model is utilized to automatically tune a full state feedback controller. This results in an improved converter performance in terms of overshoots, undershoots, and settling times. Subsequently, the SI and tuning concepts are extended in order to support the SMC law presented in this work.

Finally, a fast and low-complexity natural frequency estimation concept for switched-mode power supplies (SMPSs) is introduced. Neither a high resolution analog-to-digital converter (ADC) nor complex arithmetic operations, such as multiplications, are required by this novel method. The approach is based on the exploitation of the mismatch between the on-time of the control signal and the effective on-time at the switching node.
ZUSAMMENFASSUNG


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AC     alternating current
ADC    analog-to-digital converter
ALS    approximate linear least squares (LLS)
ASIC   application-specific integrated circuit
BD     body diode
BLS    batch LLS
CT     continuous time
DCR    direct current resistance
DC     direct current
DPWM   digital pulse-width modulation (PWM)
DS     drain-source
DT     discrete time
EMI    electromagnetic interference
ERLS-DCD exponentially weighted recursive least squares (RLS) (ERLS) with dichotomous coordinate descent
ERLS   exponentially weighted RLS
ESR    equivalent series resistance
FIR    finite impulse response
FPGA   field-programmable gate array
FSF    full state feedback
GPIO   general purpose input/output
HS     high-side
IIR    infinite impulse response
ILS    iterative LLS
I      integral
KCL    Kirchhoff’s current law
KVL  Kirchhoff’s voltage law
LDO  low-dropout regulator
LFSR linear-feedback-shift register
LLS  linear least squares
LPF  low-pass filter
LQR  linear-quadratic regulator
LS   low-side
LSB  least significant bit
LTI  linear time-invariant
MOSFET metal oxide semiconductor field effect transistor
NMOS n-channel metal oxide semiconductor field effect transistor (MOSFET)
ODE  ordinary differential equation
OS   oversampling
P    proportional
PCB  printed circuit board
PID  proportional-integral-derivative
PI   proportional-integral
PMOS p-channel MOSFET
PRBS pseudorandom binary sequence
PWM  pulse-width modulation
R-SALS randomized step-adaptive approximate LLS (ALS) (SALS)
RHS  right-hand side
RLS  recursive least squares
RMS  root mean square
SALS step-adaptive ALS
SI   system identification
SMC  sliding mode control
SMO  sliding mode observer
SMPS  switched-mode power supply
SPDT  single pole double throw
SR    set-reset
SSA   state-space averaging
TF    transfer function
TFM   transfer function (TF) matrix
VRM   voltage regulator module
VSS   variable structure system
ZOH   zero-order hold
1.1 POWER CONVERSION

Energy efficiency and power consumption are important key figures of most of today’s electronic devices. On the one hand, advances, e.g., in semiconductor technologies and in the development of new hardware architectures can improve the energy efficiency of these devices. On the other hand, due to the request for new features, the overall power consumption is usually ever increasing. Most of these electronic devices contain one or more DC-DC converters. These converters generate the direct current (DC) voltage levels required by the various subsystems of the device from the input DC voltage, e.g., provided by a battery. In practice, many different possibilities are available in order to obtain the necessary DC voltages [1]. Broadly speaking, three categories can be identified [2]–[4]. These are low-dropout regulators (LDOs), switched capacitor converters, and switched-mode power supplies (SMPSs). Depending on the requirements such as performance, protection, features, and cost, one of the three types has to be selected by the designer [5]. Although SMPSs are usually more expensive than the other two solutions, their better efficiency at high load currents renders them an attractive option in many applications. Figure 1.1 outlines the basic structure of an SMPS. From the figure, the three main parts of an SMPS can be identified:

- A power stage, which is comprised of semiconductor switches such as power metal oxide semiconductor field effect transistors (MOSFETs)
- Passive filters with energy storage elements, e.g., inductors
- A controller, implemented in the analog, digital or mixed-signal domain

Typical application scenarios of SMPSs are voltage regulator modules (VRMs) for microcontrollers and microprocessors. Caused by an ever increasing amount of desired features in modern applications, the power consumption of microcontrollers and microprocessors is rapidly growing. Hence, DC-DC converters have to provide the required energy with minimum losses in order to maximize efficiency and reduce generated heat. One possibility to improve conversion efficiency at high output powers is to employ interleaved multi-phase SMPSs [6]–[9]. By using multiple parallel power stages and inductors,
the current per phase is reduced. Consequently, caused by lower conduction losses, efficiency is improved [8], [10]. Furthermore, in an interleaved topology, the pulse-width modulation (PWM) signals of the individual power stages are phase shifted with respect to each other [11]–[13]. Thus, the effective switching frequency increases, which in turn reduces both output voltage and current ripples, and potentially improves the dynamic performance [13], [14].

1.2 MOTIVATION AND TECHNICAL CHALLENGES

Regardless of operating conditions, such as line and load variation, DC-DC converters have to provide a well-regulated output voltage. Hence, a control loop is an essential part of such a converter [2], [15]. Therefore, the strong research interest in fast and robust control laws is evident. In [14], [15], it has been shown that the dynamic performance of a converter can be significantly improved if a variable switching frequency is tolerable during transient events. One method to achieve optimal dynamic behavior is time-optimal control [16], [17]. Typically, such a control scheme comprises a linear feedback loop for steady state operation and a fast acting, interrupt-based logic ensuring optimal responses to detected transients. Although such a control can offer excellent dynamic performance, switching between two control laws increases the risk of instability.

Sliding mode control (SMC) is a widely used nonlinear control law offering excellent dynamic performance, as well as high robustness, with respect to parameter variations and disturbances [18]–[21]. Due to their switching nature, DC-DC converters are inherently variable structure systems (VSSs) [22]. Therefore, SMC embodies a natural control law choice, since it is based on the large-signal representation.
of the converter [20], [23]. Furthermore, the simple design procedure is another key advantage of SMC [24]. Various SMC implementations, both analog and digital, have been successfully implemented for different converter topologies such as buck, boost and buck-boost [24]–[29].

In this work, an innovative digital SMC approach for interleaved multi-phase converters is proposed. In order to achieve a constant switching frequency and the required phase shift for interleaving between the phases, a novel hysteresis modulation control law is suggested. In contrast to state-of-the-art methods, the presented control technique does not impose any constraints on the number of required phases to achieve a specific output voltage. Furthermore, current sensing is not required in the proposed approach. Hence, the amount of required hardware can be reduced, since no current analog-to-digital converters (ADCs) are needed. Rather, a digital sliding mode observer (SMO) is introduced in order to digitally reconstruct the alternating current (AC) components of the inductor currents, which are required by the SMC law.

In many application scenarios, different configurations of the SMPS have to be supported by a single controller. Typically, the same controller has to be reused for various distinct sets of passive components with, e.g., different inductance and capacitance values [30]. This demanded flexibility poses a significant challenge for the control design, since the system has to be stable and has to operate inside the specifications over all operating conditions for all configurations. On top of that, components tolerances and other effects, such as aging, may have a negative impact on the system’s performance [31], [32]. Thus, it would be desirable to identify the dynamics of the plant, and tune the controller accordingly [33]. To accomplish this task, various system identification (SI) approaches have been proposed in literature [34]–[40]. Nevertheless, the required computational complexity often hinders the implementation of many of these SI methods in an actual product [41]. Therefore, another focus of this work is the investigation and development of low-complexity SI concepts for SMPSs that are suitable for an implementation in digital hardware. Consequently, a state-space-based parametric SI concept is introduced, which features less computational complexity than state-of-the-art solutions, while achieving a better estimation accuracy. Additionally, a non-parametric SI method is presented in this work. While the scope of this method is limited in comparison to parametric approaches, i.e., only an estimate of the natural frequency of the converter is obtained, its highly efficient implementation renders it a promising approach for a practical implementation of an SI approach in the low cost segment.
1.3 ORGANIZATION OF THIS WORK

The rest of this work is structured as follows: Chapter 2 reviews the basic principles of SMPSs and multi-phase DC-DC converter topologies. The large- and small-signal models of a multi-phase buck converter are also derived. Furthermore, a brief overview of the state of the art of digital control, SMC, and SI for multi-phase DC-DC converters is given. This prepares the way for Chapter 3, which covers a novel SMC theory based control concept for multi-phase DC-DC converters. Subsequently, the design of a digital controller for multi-phase DC-DC converters, which achieves fixed-frequency and interleaved operation in steady state, is carried out. To that end, a variable hysteresis SMC is proposed. In Chapter 4, an innovative SMO state estimation method for the SMC laws addressed in Chapter 3 is presented. Different SI approaches and their application to SMPSs are introduced in Chapter 5. Moreover, SI based controller tuning methods are discussed. Implementation details of the proposed digital control concepts and SI approaches are presented in Chapter 6 followed by the corresponding experimental results in Chapter 7. Chapter 8 concludes this thesis and suggests promising topics for further research.

1.4 CONTRIBUTIONS

During the work on this thesis the following scientific contributions have been published in peer reviewed conference proceedings and journals or have been filed as patents. Some ideas and figures presented in this thesis previously appeared in these publications and patents:


Additionally, the following manuscripts have been submitted to peer reviewed journals and are currently under review:


The digital control concepts for multi-phase DC-DC converters proposed in this work cover multiple subjects such as power electronics, control theory, and estimation theory. In order to comprehend the design process more easily, an introduction to the involved theories and disciplines is given in this chapter. The state of the art of these subjects with respect to DC-DC converters is also summarized. Firstly, the basic operation principle of SMPSs is reviewed based on the example of a buck converter. Then, the fundamentals of the multi-phase topology and its advantages are outlined. Large-signal models, small-signal models, and control concepts for multi-phase buck converters are derived in the following. Secondly, a brief introduction to SMC theory is given. The main idea of this non-linear control law is covered and its suitableness for DC-DC converters is emphasized. Finally, a synoptic view of SI is provided. Differences between parametric and non-parametric approaches are discussed and linear least squares (LLS) estimation is reviewed.

2.1 Fundamentals of DC-DC Conversion

As schematically shown in Figure 2.1, the objective of DC-DC converters is to supply a load with a stable output DC voltage $V_{out}$ derived from an input DC voltage $V_{in}$, e.g., provided by a battery. A trivial solution for obtaining a lower output than input voltage, i.e., $V_{out} < V_{in}$, is illustrated in Figure 2.2. For this example, a purely resistive load $R_l$ is assumed. Employing a variable resistor $R$, the output voltage can be adjusted by controlling the value of $R$. Implementing this variable resistor with a transistor, whose transconductance is regulated by a feedback loop, yields a simple LDO. Obviously, the power loss at the transistor constitutes a negative impact on efficiency, especially if the conversion ratio $M := \frac{V_{out}}{V_{in}}$ is small. Suppose now that an application
Figure 2.2: Schematic of a resistive divider, an example of a simple DC-DC converter.

requires an output voltage of \( V_{\text{out}} = M V_{\text{in}} \). By applying the voltage divider rule, the required value of \( R \) can be readily calculated to be

\[
R = \frac{R_l V_{\text{in}}}{V_{\text{out}}} - R_l = \frac{R_l}{M} - R_l. \tag{2.1}
\]

Furthermore, since the input power is given as

\[
P_{\text{in}} = V_{\text{in}} I_l = P_R + P_{\text{out}} = I_l^2 R + V_{\text{out}} I_l, \tag{2.2}
\]

a conversion efficiency of

\[
\eta := \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{V_{\text{out}} I_l}{V_{\text{in}} I_l} = \frac{V_{\text{out}}}{V_{\text{in}}} = M \tag{2.3}
\]

is achieved by such a circuit. If, e.g., an output voltage of \( V_{\text{out}} = 0.5 V_{\text{in}} \) is required, 50 % of the input power is dissipated at \( R \), yielding a conversion efficiency of only \( \eta = 0.5 \). Since high power losses are unacceptable in many applications, different DC-DC conversion approaches are often required.

Such an alternative solution to DC-DC conversion is provided by so called SMPSs. These converters typically employ switches to toggle between different circuit subtopologies. Such converters, assuming ideal components, achieve 100 % efficiency. In other words, they operate lossless. While various kinds of SMPSs exist for step-down, step-up, and step-up/step-down conversion, this work focuses on the buck topology, i.e., step-down converters.

2.2 Switched-Mode Power Supplies

In Figure 2.3a, the basic buck converter topology is reported. Its purpose is to step an input voltage \( V_{\text{in}} \) down to an output voltage \( V_{\text{out}} \). The converter comprises an inductor and a capacitor with inductance \( L \) and capacitance \( C \), respectively. The voltage drops across \( L \) and \( C \) are denoted by \( v_L(t) \) and \( v_C(t) \), while the currents through them are given by \( i_L(t) \) and \( i_C(t) \). Furthermore, \( i_{\text{in}}(t) \) and \( i_l(t) \) mark the input and the load current, respectively. Finally, a single pole double throw (SPDT) switch, toggled by the control signal \( c(t) \), is required.
2.2 SWITCHED-MODE POWER SUPPLIES

The voltage across the switch, commonly referred to as the switching node voltage, is denoted by $v_{sw}(t)$. As depicted in Figure 2.3b and Figure 2.3c, the position of the switch determines the active configuration. Basically, by controlling the SPDT switch with the PWM signal $c(t)$, having a duty cycle $D$ and a switching period $T_{sw}$, the switching node voltage $v_{sw}(t)$ exhibits a rectangular waveform. The second-order $LC$ low-pass filter (LPF) then filters $v_{sw}(t)$ in order to obtain the (approximately) constant output voltage $v_{out}(t)$. This is the fundamental idea of an SMPS.

The typical steady state waveforms of a buck converter are illustrated in Figure 2.4. During the on-time $T_{on}$ (Figure 2.3b), $V_{in}$ is connected to the switching node and the inductor current $i_L(t)$ increases. Conversely, during the off-time $T_{off}$ (Figure 2.3c), the switching node is connected to ground and hence, $i_L(t)$ decreases. As a consequence, the input current $i_{in}(t)$ exhibits a discontinuous waveform, and is only nonzero during the on-time, where it equals $i_L(t)$.

As shown in Figure 2.4, all currents and voltages of the converter are periodic during steady state, with a period equal to the switching period $T_{sw}$. The objective of steady state analysis is now to derive expressions for the converter’s state variables and outputs in terms of its inputs. This can be accomplished by utilizing two basic principles, which directly follow from the periodic nature of the voltages and currents. Firstly, as anticipated by the shaded area of the $v_{L}(t)$ curve in Figure 2.4, the average inductor voltage over a switching period is zero, i.e., no net change of the magnetic flux takes place. This is known as the inductor volt-second balance and can be written as

$$\langle v_{L}(t) \rangle_{T_{sw}} = \frac{L}{T_{sw}} (i_L(t + T_{sw}) - i_L(t)) = 0. \quad (2.4)$$

Note that, the moving average operator $\langle \cdot \rangle_{T}$ in (2.4) is defined as

$$\langle f(t) \rangle_{T} := \frac{1}{T} \int_{t}^{t+T} f(\tau) \, d\tau. \quad (2.5)$$

An akin principle can be applied to the capacitor current $i_C(t)$. Caused by the periodic capacitor voltage $v_C(t)$, the charge delivered by and stored to the capacitor even out and hence the average capacitor current is zero. This second principle, expressed as

$$\langle i_C(t) \rangle_{T_{sw}} = \frac{C}{T_{sw}} (v_C(t + T_{sw}) - v_C(t)) = 0, \quad (2.6)$$

is called capacitor ampere-second balance.

With the two presented principles, it is possible to obtain the steady state solution of the SMPS. As a first step, by applying conventional circuit analysis, expressions for the converter’s waveforms during the two different configurations are derived. During the subinterval $[0, DT_{sw}]$, which defines the on-time $T_{on} := DT_{sw}$, the voltage across the inductor $L$ is given by

$$V_{L,T_{on}} = V_{in} - V_{C}. \quad (2.7)$$
Figure 2.3: Schematic of a buck converter, an example of an SMPS. The different positions of the switch result in two distinct converter configurations.
Figure 2.4: Exemplary waveforms of a buck converter during steady state operation.
Here, by using the small-ripple approximation, $v_C(t)$ has been replaced by its DC value $V_C$. In other words, the switching ripple $\Delta v_C(t)$ is neglected for calculating the voltage over the inductor. This approximation greatly simplifies the derivation of the steady state solution and is well met in many practical converters. Then, for the second subinterval $[DT_{sw}, T_{sw}]$, which determines the off-time $T_{off} := D'T_{sw} := (1 - D) T_{sw}$, the inductor voltage is found to be

$$V_{L, t_{off}} = -V_C. \tag{2.8}$$

In a similar fashion, the capacitor current during $T_{on}$ and $T_{off}$ can be expressed as

$$I_{C, T_{on}} = I_{C, t_{off}} = I_L - I_I. \tag{2.9}$$

Then, from the inductor volt-second balance (2.4)

$$\langle v_L(t) \rangle_{T_{sw}} = DV_{L, T_{on}} + D'V_{L, T_{off}} = D (V_{in} - V_C) - (1 - D) V_C$$

$$= DV_{in} - V_C = 0$$

$$\implies V_C = DV_{in}, \tag{2.10}$$

and the capacitor ampere-second balance (2.6)

$$\langle i_C(t) \rangle_{T_{sw}} = DI_{C, T_{on}} + D'I_{C, T_{off}} = D (I_L - I_I) + (1 - D) (I_L - I_I)$$

$$= I_L - I_I = 0$$

$$\implies I_L = I_I, \tag{2.11}$$

the steady state DC components $V_C$ and $I_L$ of the capacitor voltage and inductor current, respectively, are readily obtained. Furthermore, the voltage conversion ratio can be calculated from (2.10) as

$$M(D) := \frac{V_{out}}{V_{in}} = \frac{V_C}{V_{in}} = D. \tag{2.12}$$

With the steady state quantities available, the inductor current ripple $\Delta i_L$ and the capacitor voltage ripple $\Delta v_C$ can be estimated. As anticipated from Figure 2.4, integrating $v_L(t)$ over either of the two subintervals yields the peak-to-peak inductor current ripple

$$\Delta i_L = \Delta i_C = \frac{1}{L} \int_0^{DT_{sw}} v_L(\tau) \, d\tau = \frac{V_{L, T_{on}}}{L} D T_{sw}, \tag{2.13}$$

Since, in general, the capacitor voltage ripple $\Delta v_C$ is not symmetric, the minimum and maximum values of $v_C(t)$, occurring at $(k + \frac{D}{2}) T_{sw}$ and $(k + D + \frac{D'}{2}) T_{sw}$, respectively, have to be considered separately. Thus, $\Delta v_C$ calculates to

$$\Delta v_C = \frac{1}{C} \left( \int_0^{D'T_{sw}} |i_C(\tau)| \, d\tau + \int_0^{D'T_{sw}} |i_C(\tau)| \, d\tau \right)$$

$$= \frac{1}{C} \left( \frac{V_{L, T_{on}}}{L} \frac{(DT_{sw})^2}{8} - \frac{V_{L, T_{off}}}{L} \frac{(D'T_{sw})^2}{8} \right). \tag{2.14}$$
The basic considerations reviewed in this section also hold for other types of SMPSs, and steady state analysis can be carried out in an analogous way as for the buck converter. Such different topologies are obtained by rearranging, or adding, or both, switches and passive elements. Examples of other SMPSs include the boost converter for step-up and the buck-boost converter for both step-down and step-up conversion.

This work focuses on a special derivative of the standard buck converter, namely, the multi-phase topology. In recent years, the popularity of this converter type has constantly increased. Its main advantages over the conventional buck converter, such as a reduced output voltage ripple, improved transient performance, and potentially higher conversion efficiency, is outlined in the following sections.

2.2.1 Multi-phase converters

In Figure 2.5, the schematic of a typical N-phase buck converter is depicted. In contrast to the conventional buck converter, the SPDT switch and the inductor are replicated \((N - 1)\) times, whereas a single output capacitor is employed. Therefore, the load current \(i_L(t)\) is divided between the \(N\) phases, whereas the input to output voltage conversion ratio is still given by \(2^{1/2}\). Typically, in order to fully exploit the
advantages of the multi-phase topology, the SPDT switches are controlled by the time-interleaved input signals \( c_{1,2,...,N}(t) \). To be more precise, depending on the number of phases \( N \), a phase shift of

\[
\varphi(N) = \frac{2\pi}{N}
\]  

is introduced between the control signals \( c_{n+1}(t) \) and \( c_n(t) \) of two adjacent phases \( (n+1) \) and \( n \). In Figure 2.6, exemplary steady state waveforms of a two-phase buck converter with interleaved control signals are illustrated. Note that, \( i_C(t) \) is equivalent to the AC component of the summed up inductor currents

\[
i_L(t) = \sum_{n=1}^{N} i_{L_n}(t).
\]  

While (2.16) is a general result for the multi-phase topology, a decrease in the ripples \( \Delta i_C \) and \( \Delta v_C \) is only achieved by interleaved
control signals. By applying the principles introduced for the single-phase converter, steady state analysis can be carried out without conceptional difficulty. The DC value $V_C$ of the capacitor voltage $v_C(t)$ and the conversion ratio $M(D)$ yield the same results as calculated in (2.10) and (2.12) for the single-phase buck converter. Contrary to that, the DC component $I_{L_n}$ of the inductor current in the $n^{th}$ phase depends on $N$. With the capacitor current given as

$$I_{C,T_{on}} = I_{C,T_{off}} = I_L - I_I = \sum_{n=1}^{N} I_{L_n} - I_I,$$

and the capacitor ampere-second balance (2.6)

$$\langle i_C(t) \rangle_{T_{sw}} = DI_{C,T_{on}} + D'I_{C,T_{off}}$$
$$= D \left( \sum_{n=1}^{N} I_{L_n} - I_I \right) + (1 - D) \left( \sum_{n=1}^{N} I_{L_n} - I_I \right)$$
$$= \sum_{n=1}^{N} I_{L_n} - I_I = 0$$

$$\Rightarrow \sum_{n=1}^{N} I_{L_n} = I_I = NI_{L_a} \ \forall n \in \{1, 2, \ldots, N\},$$

the DC components of the phase currents are obtained. Hence, the load current is equally shared between the phases. This is one important property of multi-phase converters. For this derivation, it has been assumed that all phases are equal, i.e., matching inductors are used and a common duty cycle $D$ is applied to all control signals $c_{1,2,\ldots,N}(t)$. As will be later discussed in more detail, equal current sharing may not be guaranteed without employing some kind of current balancing control.

Moreover, as highlighted by the capacitor current waveform in Figure 2.6, the effective switching frequency is $N$ times higher than that of a single-phase converter. While the load current sharing is an inherent property of multi-phase converters, the increased effective switching frequency stems from the time-interleaved operation. Since each individual phase is still operated with the switching frequency $f_{sw} = \frac{1}{T_{sw}}$, the magnitude of the inductor current ripple $\Delta i_L$ can be calculated by (2.13). Contrary to that, due to the increased effective switching frequency, the waveform of the capacitor current $i_C(t)$ changes. This in turn affects the capacitor voltage waveform and hence the magnitude of $\Delta v_C$.

In order to calculate $\Delta v_C$, an expression for $\Delta i_C$ is derived first. Consider a two-phase buck converter with $D < 0.5$, i.e., the two phases are never in the "on" state simultaneously. For such a scenario, as depicted in Figure 2.6, $\Delta i_C$ can be obtained by integrating the inductor
current slopes $\frac{v_{L,1}(t)}{L_1}$ and $\frac{v_{L,2}(t)}{L_2}$ over $T_{on}$ for either of the two phases and summing the results, yielding

$$\Delta i_C (D < 0.5, N = 2) = \sum_{n=1}^{2} \left( \frac{1}{L_n} \int_0^{T_{sw}} v_{L_n} (\tau) \, d\tau \right)$$

$$= \frac{V_{L,T_{on}}}{L} T_{sw} - \frac{V_{L,T_{off}}}{L} T_{sw}$$

$$= \frac{V_{in} - 2V_{out}}{L} T_{sw}.$$  \hfill (2.19)

Otherwise, if $D > 0.5$, the control signals $c_1(t)$ and $c_2(t)$ are simultaneously 1 for the fraction $(D - \frac{1}{2})$ of the switching period $T_{sw}$. Therefore, $\Delta i_C$ can be obtained by

$$\Delta i_C (D > 0.5, N = 2) = \sum_{n=1}^{2} \left( \frac{1}{L_n} \int_0^{T_{sw} - \frac{T_{sw}}{2}} v_{L_n} (\tau) \, d\tau \right)$$

$$= \frac{V_{L,T_{on}}}{L} \left( T_{sw} - \frac{T_{sw}}{2} \right)$$

$$+ \frac{V_{L,T_{on}}}{L} \left( T_{sw} - \frac{T_{sw}}{2} \right)$$

$$= 2 V_{in} - V_{out} \left( T_{sw} - \frac{T_{sw}}{2} \right).$$ \hfill (2.20)

Generally, for an $N$-phase converter, with the floor function denoted by $\lfloor \cdot \rfloor$,

$$N_{on} := \lfloor ND \rfloor + 1,$$ \hfill (2.21)

and

$$N_{off} := \lfloor ND' \rfloor + 1$$ \hfill (2.22)

determine the number of simultaneous phases in the "on" and "off" states during the interval $[0, \frac{T_{sw}}{N}]$, respectively [12], [13]. Furthermore, the durations of such "on" and "off" state overlaps calculate to

$$T_{N_{on}} := T_{sw} \left( D - \frac{\lfloor ND \rfloor}{N} \right),$$ \hfill (2.23)

and

$$T_{N_{off}} := T_{sw} \left( D' - \frac{\lfloor ND' \rfloor}{N} \right).$$ \hfill (2.24)

Finally, generalizing (2.19)-(2.20), and considering (2.23), gives the unified expression

$$\Delta i_C = \sum_{n=1}^{N} \left( \frac{1}{L_n} \int_0^{T_{N_{on}}} v_{L_n} (\tau) \, d\tau \right)$$

$$= \left( \frac{V_{L,T_{on}}}{L} N_{on} + \frac{V_{L,T_{off}}}{L} (N - N_{on}) \right) T_{N_{on}}$$ \hfill (2.25)
for the capacitor current ripple of an \( N \)-phase converter.

Another benefit of multi-phase converters can be deduced from (2.25). That is, the maximum achievable positive and negative current slopes of \( i_L(t) \) are \( N \) times higher than in a single-phase converter. Hence, load current changes can be satisfied in less time, which in turn improves the transient performance, as seen in Section 2.2.4.

Next, considering the "on" and "off" state overlaps, the capacitor voltage ripple \( \Delta v_C \) can be calculated. Similar to the single-phase converter, the minima and maxima of \( v_C(t) \) occur at \( T_{i\text{on}} \) and \( T_{i\text{off}} \), yielding the capacitor voltage ripple

\[
\Delta v_C = \frac{1}{C} \left( \int_0^{T_{i\text{on}}} |i_C(\tau)| \, d\tau + \int_0^{T_{i\text{off}}} |i_C(\tau)| \, d\tau \right) = \frac{1}{8C} \left( \frac{V_{L,T_{i\text{on}}}}{L} N_{\text{on}} + \frac{V_{L,T_{i\text{off}}}}{L} (N - N_{\text{on}}) \right) T_{i\text{on}}^2 \tag{2.26}
\]

\[
= \frac{1}{8C} \left( \frac{V_{L,T_{i\text{off}}}}{L} N_{\text{off}} + \frac{V_{L,T_{i\text{on}}}}{L} (N - N_{\text{off}}) \right) T_{i\text{off}}^2.
\]

The capacitor current and voltage AC ripples \( \Delta i_C \) and \( \Delta v_C \) as functions of the duty cycle \( D \) and the number of phases \( N \) are illustrated in Figure 2.7. The ripple magnitudes have been normalized with respect to the maximum value of a single-phase converter, occurring at \( D = 0.5 \). A significant decrease in the ripple amplitudes of an \( N \)-phase converter in comparison to a single-phase converter is clearly visible. Moreover, cancellation occurs for some particular combinations of \( D \) and \( N \). To be more precise,

\[
\Delta i_C = \Delta v_C = 0, \text{ if } D = \frac{n}{N} \quad \forall n \in \{0, 1, \ldots, N\}. \tag{2.27}
\]

As shown in Figure 2.6, interleaving also increases the fundamental frequency of the input current \( i_{\text{in}}(t) \) by a factor of \( N \), while simultaneously reducing its peak value. Thus, electromagnetic interference (EMI) is lower, ensuing that less expensive and smaller input filters can be employed.

Furthermore, in addition to the already discussed advantages, multi-phase converters may achieve better conversion efficiency. Up to now, only ideal converters, i.e., achieving an efficiency of \( \eta = 1 \), have been considered. In order to highlight the benefits of multi-phase converters with respect to conversion efficiency, the most important loss mechanisms in real world SMPSs are outlined in the next section.

### 2.2.2 Conversion efficiency

Typically, in order to reduce the amount of wasted energy, highly efficient SMPSs are demanded. Besides the costs savings due to less
Figure 2.7: Peak-to-peak values of the capacitor current and voltage ripples $\Delta i_C$ and $\Delta v_C$, respectively, for different duty cycles and number of phases.
dissipated energy, an increased efficiency is also beneficial since thermal stress is reduced. This in turn may result in a smaller chip area or an increased device lifetime. Moreover, battery lifetime of mobile applications may be improved. As already discussed, ideal SMPSs, such as the ones depicted in Figure 2.3 and Figure 2.5, are lossless. Hence, they achieve an efficiency of $\eta = 1$. Since a real world SMPS exhibits nonidealities, the efficiency of a practical implementation is below 100% ($\eta < 1$).

In Figure 2.8, a possible implementation of an $N$-phase synchronous buck converter is depicted. Each SPDT switch is implemented with a pair of MOSFETs: a p-channel MOSFET (PMOS) (high-side (HS) switch) and an n-channel MOSFET (NMOS) (low-side (LS) switch) for the connection to the input voltage and ground, respectively. Note that, the body diodes (BDs) of the MOSFETs are explicitly reported in the figure. In contrast to the ideal converter illustrated in Figure 2.5, Figure 2.8 additionally includes the main parasitic components. The direct current resistance (DCR) of the power inductor in the $n^{th}$ phase is denoted by $R_{Ln}$, while the equivalent series resistance (ESR) of the common output capacitor is given by $R_C$. Furthermore, the HS and LS switches exhibit undesired parasitic resistances $R_{HSn}$ and $R_{LSn}$, respectively, when conducting. The SPDT switches can also be realized by replacing
the LS switches with free-wheeling diodes, yielding an asynchronous converter.

Before discussing the loss mechanisms in a nonideal SMPS, it is beneficial to investigate the steady state behavior of such a real world converter. Considering the parasitic resistances and utilizing the small ripple approximation, the inductor voltages of the converter depicted in Figure 2.8 calculate to

\[ V_{L_n,T_{on}} = V_{in} - V_{out} - I_{L_n} (R_{HS_n} + R_{L_n}), \] (2.28)

and

\[ V_{L_n,T_{off}} = -V_{out} - I_{L_n} (R_{LS_n} + R_{L_n}), \] (2.29)

during \( T_{on} \) and \( T_{off} \), respectively. Thus, by applying the inductor voltage-second balance from (2.4), the voltage conversion ratio \( M(D_n) \) is obtained as

\[
\langle v_{L_n}(t) \rangle_{T_{sw}} = D_n V_{L_n,T_{on}} + D'_n V_{L_n,T_{off}} \\
= D_n (V_{in} - V_{out} - I_{L_n} (R_{HS_n} + R_{L_n})) \\
- (1 - D_n) (V_{out} + I_{L_n} (R_{LS_n} + R_{L_n})) \\
= D_n (V_{in} + I_{L_n} (R_{LS_n} - R_{HS_n})) \\
- I_{L_n} (R_{LS_n} + R_{L_n}) - V_{out} = 0
\]

\[ \implies M(D_n) := \frac{V_{out}}{V_{in}} = D_n \left(1 + \frac{I_{L_n}}{V_{in}} (R_{LS_n} - R_{HS_n})\right) \]

\[ -\frac{I_{L_n}}{V_{in}} (R_{L_n} + R_{LS_n}). \] (2.30)

Note that, there is only one conversion ratio in a multi-phase converter, even in the presence of different parasitic resistances in the phases. This is expected, since the current in a phase is inversely proportional to its resistance if the same duty cycle \( D \) is applied to all phases [42]. A similar conclusion can be drawn for the case of different duty cycles. This may also cause an unequal sharing of the load current, but \( \frac{V_{out}}{V_{in}} \) stays the same for all phases. Nevertheless, in contrast to an ideal converter, the conversion ratio now depends on the number of phases \( N \) and the load current \( I_L \). This result is anticipated, since the voltage drops over the parasitic resistances increase with \( I_L \) and decrease with \( N \). Furthermore, from (2.28)-(2.29) it directly follows that the inductor current slopes differ from that of an ideal converter. Hence, the peak-to-peak current ripples \( \Delta i_L \) and \( \Delta i_C \), as well as the capacitor current ripple \( \Delta v_C \), differ from an ideal converter. Nevertheless, (2.13) and (2.25), are still valid for calculating the current ripples. Contrary to that, because of the additional voltage drop over the parasitic resistance \( R_C \) of the output capacitor, \( v_{out}(t) = v_C(t) \) no longer holds. With the peak-to-peak amplitude of the current flowing through \( R_C \) given by \( \Delta i_C \), the output voltage ripple can be approximated as

\[ \Delta v_{out} \approx \Delta v_C + \Delta i_C R_C. \] (2.31)
With the steady state analysis of a lossy converter finished, its efficiency can now be determined. The most important conversion losses can be divided into two categories, namely, conduction and switching losses. Typically, conduction losses dominate for high output currents, whereas switching losses are prevalent in the low output current area. In the following, an overview of these two loss mechanisms is given.

Conduction losses result from parasitic resistances of the active and passive components from which a DC-DC converter is built. A typical example is the \( R_{L_n} \) of a power inductor. The conduction losses caused by \( R_{L_n} \) are equal to

\[
P_{R_{L_n}} = I_{L_n,RMS}^2 R_{L_n}.
\]

Here, \( I_{L_n,RMS} \) denotes the root mean square (RMS) of the inductor current \( i_{L_n}(t) \). For the converter depicted in Figure 2.8, \( i_{L_n} \) consists of the DC component \( \frac{I_1}{N} \) and a triangular AC ripple with peak-to-peak amplitude \( \Delta i_L \) and period \( T_{sw} \). Hence, calculating the RMS value yields

\[
I_{L_n,RMS} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{sw}} (i_{L_n} (\tau))^2 d\tau} = \sqrt{\left( \frac{I_1}{N} \right)^2 + \frac{\Delta i_L^2}{12}}.
\]

Likewise, the power loss caused by the ESR of the output capacitor can be calculated as

\[
P_{R_C} = I_{C,RMS}^2 R_C.
\]

However, \( i_C(t) \) comprises an AC ripple (with peak-to-peak amplitude \( \Delta i_C \)) only and hence \( P_{R_C} \) is typically negligible in comparison to \( P_{R_{L_n}} \).

In addition to the power dissipation \( P_{R_{L_n}} \), the losses in the parasitic resistances of the HS and LS switches have to be considered. Generally speaking, if a MOSFET is turned on and is carrying the current \( i(t) \), its conduction losses are given by

\[
P_{R_{DS(on)}} = I_{RMS}^2 R_{DS(on)}.
\]

with the RMS value of \( i(t) \) denoted as \( I_{RMS} \) and the "on" resistance \( R_{DS(on)} \) of the MOSFET. Since the switches are only turned on for a fraction of the switching period, \( R_{DS(on)} \) has to be weighted accordingly. Assuming a synchronous buck converter, the combined resistive losses of the HS and LS switch can be calculated as

\[
P_{R_{DS(on)}} = D \left( I_{L_n,RMS}^2 R_{HS} \right) + D' \left( I_{L_n,RMS}^2 R_{LS} \right).
\]

From (2.36), it can be deduced that, depending on the steady state duty cycle value \( D \), one transistor can dominate \( P_{R_{DS(on)}} \). Therefore, sizing the two transistors differently can be beneficial in terms of efficiency.
If an asynchronous topology is employed, i.e., the LS switch is replaced by a diode, the diodes’ conduction losses are given by

\[ P_{D_n} = D' I_{L,n,RMS} V_F. \quad (2.37) \]

Due to the typically large voltage drop over the diode \( V_F \geq 0.3 \text{V} \), the conversion efficiency of an asynchronous converter is usually worse for higher load currents than that of a synchronous implementation.

Similar to the conduction losses of the diode in an asynchronous converter, the losses caused by the BD of the LS switch have to be considered for the synchronous implementation. In order to prevent shoot-through, i.e., simultaneous conduction of the HS and the LS switches, dead times are required. These dead times are inserted between the turn off instant of the LS switch and the turn on instant of the HS switch, and vice versa. Since neither the HS nor the LS transistor is conducting during the dead times, the current \( i_{L,n} (t) \) has to flow through the BD of the LS switch. Recalling \((2.37)\), the resulting conduction losses yield

\[ P_{BD_n} = \left( \frac{T_p + T_n}{T_{sw}} \right) I_{L,n,RMS} V_{BD,F}, \quad (2.38) \]

with the two dead times denoted by \( T_p \) and \( T_n \) and the voltage drop over the BD given as \( V_{BD,F} \).

Additional losses are caused by the switching behavior of an SMPS. The occurrence of these switching losses stems from the fact that the power transistors used for switch realization cannot toggle between the on and off state instantaneously. Instead, a finite time is required for these transitions. Energy is dissipated as the transistor is switching, since neither the voltage across the transistor nor the current through it are zero during that timespan. In Figure 2.9, the drain current \( i_{HS,D} (t) \) and drain-to-source voltage \( v_{HS,DS} (t) \) of the HS switch during a transition from the off to the on state are sketched. During the off transition, the converse behavior is observed, i.e., \( i_{HS,D} (t) \) drops and \( v_{HS,DS} (t) \) increases. From the figure and the aforementioned observation, the switching losses

\[ P_{HS,sw} = \frac{I_{L,n,RMS} V_{in}}{2} \left( \frac{T_r + T_f}{T_{sw}} \right) \quad (2.39) \]
of the HS transistor can be readily derived. In (2.39), \( T_r \) and \( T_f \) denote the time duration of the turn on and off transition, respectively. Compared to the HS switch, the LS transistor’s drain-source voltage during transition is much lower. This is caused by the conduction of its BD during the dead times. Hence, although similar considerations as (2.39) apply for the LS switch, its switching losses are usually negligible in comparison to its conduction losses.

Furthermore, the power required to charge the gate of a MOSFET, calculated as

\[
P_G = \frac{Q_G V_{DD}}{T_{sw}},\quad (2.40)
\]

causes additional switching losses. Here, the gate charge is given by \( Q_G \), and \( V_{DD} \) denotes the supply voltage of the driver circuit charging the gate. Note that, as the parasitic resistance, the gate charge can differ between the employed MOSFETs, e.g., due to manufacturing tolerances. Furthermore, different types of MOSFETs may be used for the HS and LS switches. Hence, the gate charges \( Q_{G,HS} \) and \( Q_{G,LS} \) of the HS switch and the LS switch, respectively, have to be considered separately, yielding the total gate charge loss

\[
P_{Gn} = \frac{Q_{G,HS} V_{DD,HS}}{T_{sw}} + \frac{Q_{G,LS} V_{DD,LS}}{T_{sw}},\quad (2.41)
\]

for the \( n \)th phase of a synchronous converter.

With the main loss mechanism identified, the efficiency of an \( N \)-phase synchronous buck converter finally calculates to

\[
\eta := \frac{P_{out}}{P_{in}} = \frac{V_{out} I_I}{V_{out} I_I + \sum_{n=1}^{N} \left( P_{R_{L_n}} + P_{R_{TD(n)on}} + P_{BD_n} + P_{HS_{wa}} + P_{C_n} \right) + P_{RC}}.\quad (2.42)
\]

From (2.42), it can be understood that increasing the number of phases can improve efficiency if conduction losses are the main contributor to the total power dissipation. The reason behind that is the distribution of \( I_I \) between the phases, which reduces \( I_{L_n,RMS} \) and in turn \( P_{R_{L_n}} \) and \( P_{R_{TD(n)on}} \). In contrast to that, \( P_{C_n} \) is independent of the load current and thus, due to the additional switches, gate charge losses increase proportionally to \( N \). Hence, a signal-phase converter displays a better efficiency under light load conditions. The efficiency curves plotted in Figure 2.10 support these notions.

To summarize, various converter parameters influence the efficiency. Input and output voltage are typically fixed and the RMS currents of the inductors also depend on the load requirements. In contrast to that, the switching period length, transitions times and parasitic resistances can be optimized in order to improve the conversion efficiency.
By increasing $T_{sw}$, switching losses are decreased with the downside of requiring larger $L$ and $C$ to maintain the same inductor current and output voltage ripples. Furthermore, the power MOSFETs should have a low $R_{DS(on)}$ and exhibit fast switching transients. This represents another trade-off, since $R_{DS(on)}$ decreases with area, but switching speed is proportional to the gate charge $Q_G$, which increases with area. Similarly, lowering the DCR of the inductor can be achieved by increasing the diameter of the coil wire, which may be more costly and area consuming. Additionally, in order to optimize the efficiency of multi-phase converters, techniques such as phase-shedding are often employed. Instead of always operating with all phases, the number of active phases is selected on the basis of the instantaneous current requirement of the load.

2.2.3 Modeling of switched-mode power supplies

Up to now, only the steady state operation of converters has been analyzed. In order to provide a stable and defined output voltage regardless of operating conditions, e.g., instantaneous input voltage and load current, an SMPS is usually closed-loop controlled. In other words, the control inputs are no longer constant, but calculated by a controller.

Typically, accurate converter models have to be derived in order to design fast and robust control structures. Naturally, the relationship between the control input and the system output, e.g., between the duty cycle $d_n(t)$ of $c_n(t)$ and the output voltage $v_{out}(t)$, is especially important. Moreover, the audio susceptibility, which relates the input voltage $v_{in}(t)$ to $v_{out}(t)$, and the influence of the load current $i_l(t)$
on \( v_{\text{out}}(t) \) capture other dominant dynamics of the converter. Many different modeling approaches, such as state-space averaging (SSA) [2, 43], large-signal treatment of the VSS [22], non-linear frequency-dependent methods [44], and discrete time (DT) modeling [45, 46], to only name a few, have been extensively studied in the past.

For linear controllers, such as proportional-integral-derivative (PID) compensators, a linear time-invariant (LTI) model of the system under exam is usually desired. Hence, the SSA approach and DT modeling, which yield an LTI state-space description of the converter in continuous time (CT) and DT, respectively, are particularly popular. In the following, SSA theory, following the notation used in [47], is reviewed and models for an \( N \)-phase buck converter are derived.

Considering the converter reported in Figure 2.8, an LTI model can be obtained by means of SSA. For every possible combination of switch positions, enumerated as \( i \in \{0, 1, \ldots, 2^N - 1\} \), a state-space representation

\[
\dot{x}(t) = A_i x(t) + B_i v(t), \quad (2.43a)
\]

\[
y(t) = C_i x(t) + D_i v(t), \quad (2.43b)
\]

can be readily found. In (2.43), the system, input, output and feedforward matrices are defined as \( A_i \in \mathbb{R}^{(N+1)\times(N+1)} \), \( B_i \in \mathbb{R}^{(N+1)\times(N+1)} \), \( C_i \in \mathbb{R}^{(N+2)\times(N+1)} \), and \( D_i \in \mathbb{R}^{(N+2)\times2} \). Moreover, \( x(t) \in \mathbb{R}^{(N+1)\times1} \), \( v(t) \in \mathbb{R}^{2\times1} \) and \( y(t) \in \mathbb{R}^{(N+1)\times1} \) denote the states, inputs and outputs of the plant. For the converter at hand, the state vector

\[
x(t) = \begin{bmatrix} v_C(t) \\ i_{L_1}(t) \\ i_{L_2}(t) \\ \vdots \\ i_{L_N}(t) \end{bmatrix} \quad (2.44)
\]

is composed of the voltage over the output capacitor and the inductor currents. Furthermore, the output vector

\[
y(t) = \begin{bmatrix} v_{\text{out}}(t) \\ i_L(t) \\ i_{L_1}(t) \\ i_{L_2}(t) \\ \vdots \\ i_{L_N}(t) \end{bmatrix} \quad (2.45)
\]
Table 2.1: Possible configurations of the switches for a two-phase buck converter.

<table>
<thead>
<tr>
<th>Substructure $i$</th>
<th>Position $HS_1$</th>
<th>Position $HS_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>open</td>
<td>open</td>
</tr>
<tr>
<td>1</td>
<td>closed</td>
<td>open</td>
</tr>
<tr>
<td>2</td>
<td>open</td>
<td>closed</td>
</tr>
<tr>
<td>3</td>
<td>closed</td>
<td>closed</td>
</tr>
</tbody>
</table>

comprises the output voltage, individual inductor currents and the sum of the inductor currents. Finally, assuming a current sink load, the large-signal model’s input vector can be defined as

$$v(t) = \begin{bmatrix} v_{in}(t) \\ i_L(t) \end{bmatrix}. \quad (2.46)$$

Since the $HS$ and $LS$ switches are operated complementary to each other, the four substructures listed in Table 2.1 are obtained with a two-phase converter.

Applying Kirchhoff’s voltage law (KVL) and Kirchhoff’s current law (KCL) to the configuration with both $HS$ switches open, i.e., $i = 0$, yields

$$A_0 = \begin{bmatrix} 0 & -\frac{1}{L_1} & \frac{1}{C_1} & \frac{1}{L_1} \\ -\frac{1}{L_2} & -\frac{R_{p1}+R_C}{L_1} & \frac{R_C}{L_1} & \frac{R_{p1}+R_C}{L_1} \\ -\frac{1}{L_2} & \frac{R_C}{L_2} & -\frac{R_{p2}+R_C}{L_2} & \frac{R_{p2}+R_C}{L_2} \end{bmatrix}, \quad (2.47a)$$

$$B_0 = \begin{bmatrix} 0 & -\frac{1}{C} \\ 0 & \frac{R_C}{L_1} \\ 0 & \frac{R_C}{L_2} \end{bmatrix}, \quad (2.47b)$$

$$C_0 = \begin{bmatrix} 1 & R_C & R_C \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 1 \end{bmatrix}, \quad (2.47c)$$

and

$$D_0 = \begin{bmatrix} 0 & -R_C \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad (2.47d)$$
where \( R_{p_n} := \left( R_{DS(on)n} + R_{L_n} \right) \) denotes the sum of parasitic resistances in the \( n^{th} \) phase. For the sake of brevity, as motivated in (2.36), \( R_{DS(on)n} := D_nR_{HS_n} + D_n'R_{LS_n} \) is assumed. Similarly, performing the analysis for the remaining three configurations, the system, input, output and feedforward matrices are readily obtained as

\[
A_3 = A_2 = A_1 = A_0, \quad (2.48a)
\]

\[
B_1 = \begin{bmatrix}
0 & -\frac{1}{C} \\
\frac{1}{L_1} & \frac{R_C}{L_1} \\
0 & \frac{R_C}{L_2}
\end{bmatrix}, \quad (2.48b)
\]

\[
B_2 = \begin{bmatrix}
0 & -\frac{1}{C} \\
0 & \frac{R_C}{L_1} \\
\frac{1}{L_2} & \frac{R_C}{L_2}
\end{bmatrix}, \quad (2.48c)
\]

\[
B_3 = \begin{bmatrix}
0 & -\frac{1}{C} \\
\frac{1}{L_1} & \frac{R_C}{L_1} \\
\frac{1}{L_2} & \frac{R_C}{L_2}
\end{bmatrix}, \quad (2.48d)
\]

\[
C_3 = C_2 = C_1 = C_0, \quad (2.48e)
\]

and

\[
D_3 = D_2 = D_1 = D_0. \quad (2.48f)
\]

Since the topology of the converter switches between the different subconfigurations, the system under exam is time-variant. The objective of SSA is now to obtain a time-invariant representation of the plant by neglecting the high-frequency components of the converter’s dynamics. To that end, the moving average operator, as defined in (2.5), is applied to \( \dot{x}(t) \). In other words, the average rate of change \( \langle \dot{x}(t) \rangle_{T_m} \) of the state vector is found by weighting the different configurations, given by (2.43a), according to their contribution to a sin-
gle switching period. Hence, the averaged dynamics of the converter yield

\[
\langle \dot{x}(t) \rangle_{T_{sw}} = \frac{1}{T_{sw}} \int_{0}^{T_{sw}} \dot{x}(\tau) \, d\tau
\]

\[
= \int_{0}^{d_{1}(t)} (A_{1}x(\tau) + B_{1}v(\tau)) \, d\tau
\]

\[
+ \int_{d_{1}(t)}^{1} (A_{0}x(\tau) + B_{0}v(\tau)) \, d\tau
\]

\[
+ \int_{1}^{\frac{1}{2}+d_{2}(t)} (A_{2}x(\tau) + B_{2}v(\tau)) \, d\tau
\]

\[
+ \int_{\frac{1}{2}+d_{2}(t)}^{1} (A_{0}x(\tau) + B_{0}u(\tau)) \, d\tau
\]

\[
= \underbrace{(d_{1}(t)A_{1} + d_{2}(t)A_{2} + (1 - d_{1}(t) - d_{2}(t))A_{0})}_{A_{SSA}}(x(t))_{T_{sw}}
\]

\[
+ \underbrace{(d_{1}(t)B_{1} + d_{2}(t)B_{2} + (1 - d_{1}(t) - d_{2}(t))B_{0})}_{B_{SSA}}(v(t))_{T_{sw}},
\]

\[(2.49)\]

whereby \(d_{1}(t)\) and \(d_{2}(t)\) denote the duty cycles of \(c_{1}(t)\) and \(c_{2}(t)\), respectively. Moreover, in the derivation of (2.49) a converter with a switching sequence as depicted in Figure 2.6 is presumed. To be more precise, \(d_{1}(t) < 0.5\) and \(d_{2}(t) < 0.5\) are assumed. Nevertheless, it can be easily shown that

\[
A_{SSA} := A_{0} = A_{1} = A_{2} = A_{3},
\]

\[(2.50)\]

and

\[
B_{SSA} := \begin{bmatrix}
0 & -\frac{1}{C} \\
\frac{d_{1}(t)}{L_{1}} & \frac{R_{C}}{L_{1}} \\
\frac{d_{2}(t)}{L_{2}} & \frac{R_{C}}{L_{2}} \\
\cdots & \cdots \\
\frac{d_{N}(t)}{L_{N}} & \frac{R_{C}}{L_{N}}
\end{bmatrix}
\]

\[(2.51)\]

hold regardless of the duty cycles of \(c_{1}(t)\) and \(c_{2}(t)\). In fact, for an arbitrary multi-phase buck converter with \(N\) phases, the system matrix of the large-signal averaged model is time-invariant over all configurations, i.e.,

\[
A_{SSA} := A_{0} = A_{1} = A_{2} = \cdots = A_{(2^{N}-1)},
\]

\[(2.52)\]

and the corresponding input matrix is given by

\[
B_{SSA} := \begin{bmatrix}
0 & -\frac{1}{C} \\
\frac{d_{1}(t)}{L_{1}} & \frac{R_{C}}{L_{1}} \\
\frac{d_{2}(t)}{L_{2}} & \frac{R_{C}}{L_{2}} \\
\cdots & \cdots \\
\frac{d_{N}(t)}{L_{N}} & \frac{R_{C}}{L_{N}}
\end{bmatrix}
\]

\[(2.53)\]
With $B_{SSA}$ as defined in (2.53), the duty cycles $d_{1,2,...,N}(t)$ can be interpreted as additional inputs to the system. This interpretation is meaningful, since the duty cycles are actually controlled in order to obtain the desired output voltage.

In a similar manner to (2.49), by averaging the output equations (2.43b) of an $N$-phase buck converter over $T_{sw}$, the output matrix

$$C_{SSA} := C_0 = C_1 = C_2 = C_{(2^N-1)}, \quad (2.54)$$

and the feedforward matrix

$$D_{SSA} := D_0 = D_1 = D_2 = D_{(2^N-1)}, \quad (2.55)$$

which are also time-invariant, are obtained. Hence, the averaged version of (2.43) can be written as

$$\langle \dot{x}(t) \rangle_{T_{sw}} = A_{SSA} \langle x(t) \rangle_{T_{sw}} + B_{SSA} \langle v(t) \rangle_{T_{sw}}, \quad (2.56a)$$

$$\langle y(t) \rangle_{T_{sw}} = C_{SSA} \langle x(t) \rangle_{T_{sw}} + D_{SSA} \langle v(t) \rangle_{T_{sw}}. \quad (2.56b)$$

While applying the moving average operator removes the time-varying nature of the system matrix and output equation, (2.56) is a non-linear state-space model, due to the introduction of $d_{1,2,...,N}(t)$ as additional inputs. Thus, in order to obtain an LTI description of the converter, (2.56) is linearized around a steady state operating point. By enforcing constant inputs, i.e. $\langle v(t) \rangle_{T_{sw}} = V$ in (2.56), and substituting $d_{\{1,2,...,N\}}(t)$ in (2.53) with the constants $D_{\{1,2,...,N\}}$, the steady state solutions of the states and outputs are found as

$$X = -A_{SSA}^{-1} B_{SSA} V, \quad (2.57a)$$

and

$$Y = \left( -C_{SSA} A_{SSA}^{-1} B_{SSA} + D_{SSA} \right) V. \quad (2.57b)$$

With the operating point

$$Q := \begin{bmatrix} X & Y & V & D_1 & D_2 & \cdots & D_N \end{bmatrix}^T \quad (2.58)$$

and the small-signal AC components superimposed onto it defined as

$$\dot{x}(t) := \langle x(t) \rangle_{T_{sw}} - X, \quad (2.59a)$$

$$\dot{y}(t) := \langle y(t) \rangle_{T_{sw}} - Y, \quad (2.59b)$$

$$\dot{v}(t) := \langle v(t) \rangle_{T_{sw}} - V. \quad (2.59c)$$
\[
\ddot{d}_n(t) := d_n(t) - D_n \quad \forall n \in \{1, 2, \ldots, N\},
\]

one can proceed by linearizing \((2.56)\) around \(Q\), obtaining the small-signal LTI model

\[
\dot{\tilde{x}}(t) = \left. \frac{\partial(\tilde{x}(t))_{LTI}}{\partial x(t)} \right|_Q \tilde{x}(t) + \left. \frac{\partial(\tilde{x}(t))_{LTI}}{\partial v(t)} \right|_Q \tilde{v}(t) \\
+ \sum_{n=1}^{N} \left. \frac{\partial(\tilde{x}(t))_{LTI}}{\partial d_n(t)} \right|_Q \tilde{d}_n(t)
\]

\[
= A_{SSA}|_Q \tilde{x}(t) + \left[ B_{SSA}|_Q \begin{bmatrix} 0 \\ \text{diag} \left( \frac{V_{in}}{L_1}, \frac{V_{in}}{L_2}, \ldots, \frac{V_{in}}{L_N} \right) \end{bmatrix} \right] \tilde{v}(t) \\
+ \sum_{n=1}^{N} \left. \frac{\partial(\tilde{x}(t))_{LTI}}{\partial d_n(t)} \right|_Q \tilde{d}_n(t)
\]

\[
= A \tilde{x}(t) + B \tilde{u}(t),
\]

\((2.60a)\)

\[
\dot{\tilde{y}}(t) = \left. \frac{\partial(\tilde{y}(t))_{LTI}}{\partial x(t)} \right|_Q \tilde{x}(t) + \left. \frac{\partial(\tilde{y}(t))_{LTI}}{\partial v(t)} \right|_Q \tilde{v}(t) \\
+ \sum_{n=1}^{N} \left. \frac{\partial(\tilde{y}(t))_{LTI}}{\partial d_n(t)} \right|_Q \tilde{d}_n(t)
\]

\[
= C_{SSA}|_Q \tilde{x}(t) + \left[ D_{SSA}|_Q \begin{bmatrix} 0 \\ F \end{bmatrix} \right] \tilde{v}(t) \\
+ \sum_{n=1}^{N} \left. \frac{\partial(\tilde{y}(t))_{LTI}}{\partial d_n(t)} \right|_Q \tilde{d}_n(t)
\]

\[
= C \tilde{x}(t) + D \tilde{u}(t).
\]

\((2.60b)\)

Note that, in \((2.60)\), the new augmented input vector \(\tilde{u}(t)\) is introduced, which contains the input voltage, the load current, and the duty cycles. Finally, by applying the Laplace transform to \((2.60)\), the converter’s transfer function (TF) matrix (TFM) \(G(s)\) is readily obtained from

\[
\mathcal{L}\{\tilde{y}(s)\} = \left( C (sI - A)^{-1} B + D \right) \mathcal{L}\{\tilde{u}(s)\}.
\]

\((2.61)\)
Since many control design tasks are carried out in the frequency domain, (2.61) represents an especially useful CT LTI model of the converter.

Before discussing DT models, it is beneficial to investigate the implications of the employed PWM for the dynamics of the converter. The small-signal state-space model (2.60) has been derived under the assumption that a naturally sampled PWM block is used. Such a modulator compares the instantaneous value of the modulating signal \( u(t) \), typically the output of a controller, to the sawtooth carrier \( r(t) \), which yields a duty cycle equal to

\[
d_k := \frac{u(t_k)}{V_r} \quad (2.62)
\]

of the output signal \( c(t) \) in the \( k \)th switching cycle. Here, \( V_r \) is the amplitude of \( r(t) \), and the time instant at which \( u(t) \) and \( r(t) \) intersect in the \( k \)th switching cycle is denoted by \( t_k \). Therefore, the modulator can be modeled by a constant gain of

\[
G_{PWM}(s) = \frac{1}{V_r} \quad (2.63)
\]

Figure 2.11 illustrates the relevant waveforms of naturally sampled trailing-edge PWM and the resulting control signal \( c(t) \). These kind of modulators are typically employed in conjunction with analog controllers, which usually generate a CT output signal. Hence, for such a control scheme, (2.60) and (2.61) provide accurate system descriptions.

In digitally controlled converters, which are considered in this work, uniformly sampled PWM is commonly used. In contrast to their naturally sampled counterparts, the modulating signal \( u_l \) is of DT nature and is typically updated at least once per switching period. Moreover, the CT carrier \( r(t) \) is usually emulated by a DT signal \( r_m \), updated at
the highest available rate in the system, yielding a digital PWM (DPWM) system. To be more precise,
\[ u_i := u(\ell T_s) \quad \forall \ell \in \mathbb{N}, \]  
(2.64a)

\[ r_m := r(m T_{\text{digi}}) \quad \forall m \in \mathbb{N}, \]  
(2.64b)

\[ T_{\text{digi}} \ll T_s \leq T_{\text{sw}}, \]  
(2.64c)

with the sampling period \( T_s \) and the systems’ clock period \( T_{\text{digi}} \) is presumed throughout this work. This kind of PWM introduces a delay \( T_d \) into the control loop, caused by the time difference between the update instant of \( u_i \) and its intersection with \( r_m \). Furthermore, in order to achieve interleaving, the ramp signals \( r_{nm} \) in a multi-phase converter are typically phase shifted with respect to each other. As a consequence, the delay may not be equal in all phases.

Additionally, if a digital controller is employed, a computational delay is caused by the time it takes from sampling the output voltage \( v_{\text{out}}(t) \) until \( u_i \) is calculated. In a hardware implementation of the controller the computational delay can be assumed to be negligible, i.e., much smaller than the switching period length \( T_{\text{sw}} \). In such a case, the control delay is dominated by the time difference between the instant at which \( u_i \) is available and the intersection of its zero-order hold (ZOH) reconstruction with \( r_m \). All control schemes discussed in this work have been implemented in hardware. Thus, the contribution of the computational delay to the total loop delay is not considered any further.

As illustrated in Figure 2.12 for a two-phase converter, the sampling rate \( \frac{1}{T_s} \) has a direct impact on the delay and the duty cycles of the phases. For the scenario depicted in Figure 2.12a, \( u_i \) is only updated at the beginning of a new switching period, i.e., with the rising edge of \( c_1(t) \). As a consequence, \( c_1(t) \) and \( c_2(t) \) always exhibit the same duty cycle in this example. Increasing the sampling rate by a factor of two produces two samples of \( u_i \) per switching period, as shown in Figure 2.12b. As can be seen, this can result in different duty cycle values for the phases if \( u_i \) changes during the interval \([0, \frac{T_{\text{sw}}}{2}]\). To summarize, the delay is not only determined by the oversampling (OS) ratio
\[ \text{OS} := \frac{T_{\text{sw}}}{T_s}, \]  
(2.65)

but also depends on the duty cycle and may differ for the phases.

In the small-signal limit, it can be shown that the TF of a trailing-edge DPWM for the \( n \)th phase is given by
\[ G_{\text{DPWM},n}(s) = \frac{1}{V_r} e^{-sT_d,n}, \]  
(2.66)
(a) The control signal $u_l$ is updated once per switching period ($T_{sw} = T_s$).

(b) The control signal $u_l$ is updated twice per switching period ($T_{sw} = 2T_s$).

Figure 2.12: Typical waveforms of DPWM with different sampling rates for a two-phase converter.
0.2 0.4 0.6 0.8 1

0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1

Duty Cycle D

Normalized Delay \( T_{d,n} \)

\( T_{sw} \)

\( D \)

1st Phase, OS = 1
2nd Phase, OS = 1
2nd Phase, OS = 2
2nd Phase, OS = 16

\[ T_{d,n} = \left( D_n + \frac{(n - 1)}{N} - \frac{\left\lfloor \frac{\text{OS} \left( D_n + \frac{(n - 1)}{N} \right)}{\text{OS}} \right\rfloor}{\text{OS}} \right) T_{sw}. \] (2.67)

Interestingly, this result also holds for naturally sampled PWM, since in the limit \( \lim_{\text{OS} \to \infty} T_{d,n} = 0 \) \( \forall n \in \{1, 2, \ldots, N\} \) and hence (2.66) reduces to (2.63) \[48\]. The DPWM delay occurring in a two-phase converter is depicted in Figure 2.13. The reduced delay due to the increased OS ratio can be clearly seen. Note that, for an OS ratio of 2 and 16 only \( T_{d,2} \) is shown since the delays of the two phases coincide, i.e., \( T_d = T_{d,1} = T_{d,2} \).

While the modulator delay can be easily considered with the delay element (2.66), other sampling effects, such as aliasing, are not included in the CT small-signal models (2.60) and (2.61). It has been shown that this yields inaccurate results, e.g., in the duty-cycle-to-inductor-current TF, since the effect of sampling the current waveform is not accurately captured. Therefore, DT models of the converter are required if digital control is employed. In general, the DT modeling approach can be employed in order to obtain a DT representation of the converter under exam. In contrast to the SSA approach, this method inherently accounts for sampling effects and delays such as the DPWM delay, hence, yielding an accurate DT model for digital control. Nevertheless, for converters with a time-invariant topology, accurate DT models of the control-to-output dynamics can be obtained by an appropriate discretization of the SSA result. In fact, for such converters, this yields system models that are equivalent to the direct
DT modeling results. In order for a converter to be time-invariant, all subtopologies have to be equal when all inputs are set to zero, or equivalently,

\[ A_0 = A_1 = A_2 = \cdots = A_{(2^N-1)}, \]  

(2.68)

and

\[ C_0 = C_1 = C_2 = \cdots = C_{(2^N-1)}, \]  

(2.69)

have to hold [47]. As already outlined, the multi-phase buck converter topology considered in this work fulfills this condition. From here, one can start by modeling the small-signal perturbation of the \( n \)th control signal as an impulse train, weighted by the perturbation duration in the \( k \)th switching period, i.e., [47]

\[ \bar{c}_n(t) \approx T_{sw} \sum_{i=0}^{\infty} \bar{d}_{n,i} \delta(t - iT_{sw} - T_{d,n}). \]  

(2.70)

Note that, the discussed DPWM delay appears as an additional time shift in \( \delta(t) \), determining the time difference between the sampling instant of \( u_l \) and the intersection of its ZOH reconstruction with \( r_{n,m} \). Then, substituting \( \bar{d}_{n}(t) \) in (2.60a) with the right-hand side (RHS) of (2.70) and only considering the contributions of the control inputs, yields the small-signal control-to-states system of ordinary differential equations (ODEs)

\[
\dot{x}(t) = A \dot{x}(t) + E \begin{bmatrix} \bar{c}_1(t) \\ \bar{c}_2(t) \\ \vdots \\ \bar{c}_N(t) \end{bmatrix} = A \dot{x}(t) + T_{sw} E \\
\sum_{i=0}^{\infty} \text{diag} (\delta(t - iT_{sw} - T_{d,1}), \delta(t - iT_{sw} - T_{d,2}), \ldots, \delta(t - iT_{sw} - T_{d,N})) \\
\delta(t) \\
\begin{bmatrix} d_{1,i} \\ d_{2,i} \\ \vdots \\ d_{N,i} \\ d_{i,(t)} \end{bmatrix}
\]  

(2.71)
Next, by integrating (2.71) over a single switching period, i.e.,

\[ \tilde{x} ((k+1)T_{sw}) = \Phi_{sw} \tilde{x} (kT_{sw}) + T_{sw} e^{A(k+1)T_{sw}} \]

\[ \cdot \int_{kT_{sw}}^{(k+1)T_{sw}} e^{-AT} E \sum_{i=0}^{\infty} \delta_i \left( \tau \right) \tilde{d}_i \, d\tau \]

\[ = \Phi_{sw} \tilde{x} (kT_{sw}) + T_{sw} e^{A(k+1)T_{sw}} \]

\[ \cdot \int_{kT_{sw}}^{(k+1)T_{sw}} e^{-AT} E \delta_k \left( \tau \right) \tilde{d}_i \, d\tau \]

\[ = \Phi_{sw} \tilde{x} (kT_{sw}) \]

\[ + T_{sw} e^{AT_{sw}} \left[ e^{-A T_{d,1}} e_1 e^{-A T_{d,2}} e_2 \ldots e^{-A T_{d,N}} e_N \right] \tilde{d}_k, \]

(2.72)

the sampled dynamics of the state vector perturbation \( \tilde{x}_k \) are obtained. In (2.72), \( \delta_n \) denotes the \( n \text{th} \) column of \( E \). Since \( F \) in (2.60b) is a zero matrix, the control vector \( \tilde{d}_k \) does not directly appear in the output equation. Hence, the complete DT small-signal state-space model is given as

\[ \tilde{x}_{k+1} = \Phi_{sw} \tilde{x}_k + H_{sw} \tilde{d}_k, \]

(2.73a)

\[ \tilde{y}_k = C \tilde{x}_k. \]

(2.73b)

The system description in (2.73) represents an accurate DT state-space model of time-invariant topologies, considering both sampling effects and DPWM delays. Finally, the DT TFM \( G(z) \) is obtained by \( z \)-transforming (2.73), yielding

\[ Z \{ \tilde{y} \} (z) = \left( C (zI - \Phi)^{-1} H_{sw} \right) (G(z)) (Z \{ \tilde{d} \} (z)). \]

(2.74)

In contrast to the CT TFM obtained from (2.61), \( G(z) \) only considers the duty cycles as control inputs, since \( v_{in} (t) \) and \( i_l (t) \) are still CT signals, even in a digitally controlled converter. Thus, the CT model (2.60) can be used to describe their dynamics [47].

In order to illustrate the differences between the models (2.73) and (2.60), the frequency responses of \( G(z) \) and \( G(z) \) for a two-phase buck converter are compared in Figure 2.14. The converter’s parameter are reported in Table 2.2. A DPWM as depicted in Figure 2.12a, i.e., \( T_s = T_{sw} \), and with \( T_{sw} = 0.64 \mu s \) has been assumed in both cases. Additionally, while the DPWM delays are inherently present in the DT system description, (2.66) has been used to model them for the
2.2 SWITCHED-MODE POWER SUPPLIES

Table 2.2: Two-Phase buck converter parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$</td>
<td>3.3 V</td>
<td>$L_1, L_2$</td>
<td>3.3 μH</td>
</tr>
<tr>
<td>$C$</td>
<td>20 μF</td>
<td>$R_{p1}, R_{p2}$</td>
<td>220 mΩ</td>
</tr>
<tr>
<td>$R_C$</td>
<td>10 mΩ</td>
<td>$I_i$</td>
<td>0 A</td>
</tr>
<tr>
<td>$D$</td>
<td>0.2969</td>
<td>$f_{sw} = \frac{1}{T_{sw}}$</td>
<td>1.5625 MHz</td>
</tr>
<tr>
<td>$OS$</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

CT case. As anticipated, the DPWM delays manifest as an additional phase lag at higher frequencies. For the duty-cycle-to-output-voltage TFs reported in Figure 2.14a, the frequency response of the CT model considering $G_{DPWM,DT}(s)$ almost matches the DT frequency response. Only slight differences around half the switching frequency can be observed. In contrast to that, a clear discrepancy between the CT and DT models is present in the duty-cycle-to-inductor-currents TFs shown in Figure 2.14b. Even with the DPWM delays included, aliasing effects are neglected and hence a large mismatch, especially at low frequencies, is observed. While the average inductor current does not change in the presence of a static small-signal duty cycle perturbation, the sampled value, e.g., obtained at the beginning of a switching cycle, is altered by such a perturbation. This explains the zero at the origin $s = 0$ in the CT model, which is not present in the DT model [47].

It is important to stress that the duty-cycle-to-inductor-currents TFs are especially important in multi-phase converters. As will be discussed in more detail later, they are required for designing the current balancing loops. To conclude, both sampling and delay effects cannot be neglected for a digitally controlled SMPS. Hence, the derived DT models are an important step in the design procedure of such a control scheme.

In addition to the analysis in the frequency domain, time-domain comparisons of the large-signal model (2.43) and the DT small-signal model (2.73) are shown in Figure 2.15 and Figure 2.16. In Figure 2.15, simulation results of the output voltage and total inductor current for a single-phase and a two-phase buck converter during steady state are reported. As can be seen, the outputs $v_{out,k}$ and $i_{L,k}$ of the DT model coincide with the large-signal waveforms at the sampling instants. Furthermore, the ripple reduction of the interleaved two-phase converter is clearly visible. The accuracy of the models with respect to transient events is highlighted in Figure 2.16. During a step change in $u_L$, the samples obtained from the DT model match the output of a large-signal simulation. Furthermore, as previously outlined, the faster response time of the two-phase converter, caused by the increased slope of $i_L(t)$, can be observed.
Figure 2.14: Comparison of the frequency responses of the CT and DT models for a two-phase buck converter with an OS ratio of 1.
Figure 2.15: Time-domain comparison of the \(\text{CT} \) large-signal models and the \(\text{DT} \) small-signal models of a single-phase and two-phase buck converter during steady state.
Figure 2.16: Time-domain comparison of the CT large-signal models and the DT small-signal models of a single-phase and two-phase buck converter in response to a step change in $u_l$. 

(a) Waveform of the output voltage $v_{\text{out}}(t)$ and the samples $v_{\text{out},k}$.

(b) Waveform of the summed inductor currents $i_L(t)$ and the samples $i_{L,k}$. 

- 1 Phase $v_{\text{out}}(t)$ - 1 Phase $v_{\text{out},k}$
- 2 Phases $v_{\text{out}}(t)$ - 2 Phases $v_{\text{out},k}$
- 1 Phase $i_L(t)$ - 1 Phase $i_{L,k}$
- 2 Phases $i_L(t)$ - 2 Phases $i_{L,k}$
With an accurate DT model of the converter available, one is now in the position to design a digital controller for the converter. Hence, the next section reviews the design procedures of state-of-the-art linear control approaches for multi-phase buck converters.

2.2.4 Control of DC-DC converters

As anticipated in Section 2.2.3, providing a well-regulated output voltage regardless of operating conditions is typically one of the main objectives of an SMPS. Hence, a robust control loop offering fast transient performance is an essential part of such a converter. Moreover, time-interleaving and current sharing between the phases are typical further control targets if multiple phases are employed [49]. As illustrated in Figure 2.6, time-interleaving is easily obtained in a PWM controlled converter by appropriately shifting the ramp signals.

Current sharing refers to the distribution of the load current $I_l$ between the phases. As elaborated in Section 2.2.1, for an ideal converter with identical phases, $I_l$ is equally distributed between the phases if the same steady state duty cycle is applied to them. In practice, component variations, such as different parasitic resistances, cause an imbalance in the current sharing capability. Therefore, in order to achieve the desired current sharing behavior, additional control loops are usually employed. A typical current sharing behavior is equal current sharing, i.e., even distribution of $I_l$ between all phases. This scheme, which may improve efficiency and reliability, is considered throughout this work.

In the following sections, three different digital control schemes for multi-phase buck converters are presented. Namely, a PID controller, a multi-loop $T_{on}/T_{off}$ modulation approach and a full state feedback (FSF) control are reviewed. The discussion closely follows the study conducted by the author of this thesis published in [50]. Firstly, the linear PID voltage mode controller representing a standard control approach [47] is introduced. Both analog and digital implementations have been extensively studied in literature. Hence, it serves as a reference for evaluating the performance of the other control approaches proposed in this work. Secondly, the more sophisticated $T_{on}/T_{off}$ control, which has been introduced for single-phase converters in [15], is considered. By modulating both the on-time and off-time of the control signals, this method can achieve an improved dynamic performance. Thirdly, an FSF controller, which incorporates both the output voltage and inductor currents in the calculation of the modulating signal, is discussed. Finally, all three control schemes are applied to a two-phase buck converter.
2.2.4.1 **PID Controller**

In order to regulate \( V_{\text{out}} \) to the desired output voltage \( V_{\text{ref}} \), a voltage mode controller is designed. To that end, the DT model (2.74) serves as a starting point. The basic principle of the output voltage control loop is now to calculate \( d_{n,k} \) from the output voltage error

\[
v_{c,k} := (V_{\text{ref}} - v_{\text{out,k}}).
\]  

(2.75)

As a controller template, a PID controller in parallel form, given in the \( z \)-domain as

\[
C_{d_n,v_{\text{out}}} (z) = K_{p,n} + K_{i,n} \frac{T_s z^{-1}}{1 - z^{-1}} + K_{d,n} \frac{1 - z^{-1}}{T_s}
\]  

(2.76)

is chosen. Hence, the closed-loop duty-cycle-to-output-voltage \( T \)F for the \( n^{\text{th}} \) phase is given by

\[
T_{d_n,v_{\text{out}}} (z) = \frac{C_{d_n,v_{\text{out}}} (z) G_{d_n,v_{\text{out}}} (z)}{1 + C_{d_n,v_{\text{out}}} (z) G_{d_n,v_{\text{out}}} (z)}.
\]  

(2.77)

Using, e.g., the root-locus method or a frequency compensation approach, the controller gains of (2.76) for the specified closed-loop dynamics can be readily obtained [15], [47].

In a real converter, various effects such as component tolerances or temperature differences can result in a mismatch between the phases. These mismatches then cause an unequal sharing of the load current, which in turn might have a negative impact on efficiency and reliability. Therefore, an additional current balancing controller, which ensures equal current sharing, is employed. Unlike \( v_{c,k} \), the current error

\[
i_{e,k} := \frac{i_{L,k}}{N} - i_{L_n,k}
\]  

(2.78)

has to be calculated for each phase individually. In contrast to the voltage control loop where fast dynamics are required, only the elimination of the steady state current imbalance is important. Hence, a digital proportional-integral (PI) controller given as

\[
C_{d_n,i_{L}} (z) = K_{p,c,n} + K_{i,c,n} \frac{T_s z^{-1}}{1 - z^{-1}},
\]  

(2.79)

yielding the closed-loop duty-cycle-to-inductor-current \( T \)F

\[
T_{d_n,i_{L}} (z) = \frac{C_{d_n,i_{L}} (z) G_{d_n,i_{L}} (z)}{1 + C_{d_n,i_{L}} (z) G_{d_n,i_{L}} (z)}.
\]  

(2.80)

is selected. The gains \( K_{p,c,n} \) and \( K_{i,c,n} \) can then be easily found by defining the desired dynamics of (2.80).

In Figure 2.17, an exemplary control scheme for the \( n^{\text{th}} \) phase comprising the voltage mode controller \( C_{d_n,v_{\text{out}}} (z) \) and the current balancer \( C_{d_n,i_{L}} (z) \) is reported. Note that, in the figure, the ADCs indicate the sampling of the CT waveforms.
2.2 SWITCHED-MODE POWER SUPPLIES

2.2.4.2 $T_{\text{on}}/T_{\text{off}}$ Control

In the control scheme presented in Section 2.2.4.1, only the duty cycles of the phases act as control inputs to the converter. In [15], it has been shown that the transient performance of a converter can be significantly improved by controlling the on-times and the off-times of $c_n (t)$. In this section, this $T_{\text{on}}/T_{\text{off}}$ control approach will be reviewed on the example of a multi-phase buck converter. Thus, a new small-signal model with the separate control inputs $d_{\text{on},n} (t)$ and $d_{\text{off},n} (t)$ is required. Starting by rewriting $d_n (t)$ as

$$d_n (t) = \frac{t_{\text{on},n} (t)}{t_{\text{on},n} (t) + t_{\text{off},n} (t)},$$

(2.81)

a small-signal model applicable to the $T_{\text{on}}/T_{\text{off}}$ modulation scheme can be derived. To this end, $d_n (t)$ in (2.53) is substituted by the RHS
of (2.81). Considering the new control inputs \( \tilde{I}_{on,n}(t) \) and \( \tilde{I}_{off,n}(t) \), the small-signal CT model for the \( T_{on}/T_{off} \) control follows from (2.60) as

\[
\dot{x}(t) = A\hat{x}(t) + \begin{bmatrix}
B_{SSA} & Q & E_{T_{on}T_{off}}
\end{bmatrix} B_{T_{on}T_{off}} \tilde{u}_{T_{on}T_{off}}(t),
\]

\[
\dot{y}(t) = C\hat{x}(t) + D_{T_{on}T_{off}} \tilde{u}_{T_{on}T_{off}}(t).
\]

In (2.82a),

\[
E_{T_{on}T_{off}} := \begin{bmatrix}
0 & \text{diag}(V_{in T_{off,1}}, V_{in T_{off,2}}, \ldots, V_{in T_{off,N}}) \\
0 & -\text{diag}(V_{in T_{on,1}}, V_{in T_{on,2}}, \ldots, V_{in T_{on,N}})
\end{bmatrix}^T,
\]

which is obtained by differentiating (2.56a) with respect to \( t_{on,n}(t) \) and \( t_{off,n}(t) \) and subsequent substitution of all time-varying quantities by their steady state values. Furthermore, \( A, C, \) and \( \hat{x}(t) \) are defined as for the duty cycle control small-signal modelling approach reviewed in Section 2.2.3. Note that, it is not necessary to evaluate \( D_{T_{on}T_{off}} \) since it does not enter into the small-signal DT model [47].

In order to obtain the desired DT model, the DPWM delays also have to be considered for this control scheme. In a similar fashion to (2.70), the small-signal perturbations of the actuating signal \( c_n(t) \) and its complement \( c'_n(t) := 1 - c_n(t) \) are modeled by the impulse trains

\[
c_n(t) = \sum_{i=0}^{\infty} \tilde{I}_{on,n,i} \delta(t - iT_{sw} - T_{d_{on,n}}),
\]

and

\[
c'_n(t) = \sum_{i=0}^{\infty} \tilde{I}_{off,n,i} \delta(t - iT_{sw} - T_{d_{off,n}}),
\]

respectively. As in (2.70), \( T_{d_{on,n}} \) and \( T_{d_{off,n}} \) determine the input delays of the control signals. The update instants of \( t_{on,n,i} \) and \( t_{off,n,i} \) can be different in general. Hence, the corresponding delays \( T_{d_{on,n}} \) and
have to be determined separately by substituting $D_n$ in (2.67) with $T_{\text{sw},n}$ and $T_{\text{sw},n}$. Also note that, the update frequency of the on-time and off-time may differ, yielding different OS ratios. Then, by recalculating (2.71)-(2.72) with the new control inputs $\hat{t}_{\text{on},n,i}$ and $\hat{t}_{\text{off},n,i}$, one obtains the DT small-signal model

$$
\hat{x}_{(k+1)} = \Phi_{\text{sw}} \hat{x}_k + H_{\text{sw}} \hat{t}_{\text{on},k} \hat{t}_{\text{off},k},
$$

(2.86a)

and its z-domain representation

$$
\mathcal{Z}\{\hat{y}\} (z) = \left( \frac{C (zI - \Phi)^{-1} H_{\text{sw}}}{G_{\text{sw}}(z)} \right) \begin{bmatrix} \mathcal{Z}\{\hat{t}_{\text{on}}\} (z) \\ \mathcal{Z}\{\hat{t}_{\text{off}}\} (z) \end{bmatrix}
$$

(2.87)

for $T_{\text{on}}/T_{\text{off}}$ control. Here, $\hat{t}_{\text{on},k}$ and $\hat{t}_{\text{off},k}$ are column vectors of dimension $\mathbb{R}^N$, containing the small-signal on-times $\hat{t}_{\text{on},n,k}$ and off-times $\hat{t}_{\text{off},n,k}$, respectively, of all phases.

With the derived model given in (2.87), it is now possible to design a dual-loop control strategy for the output voltage, where both the on- and off-time of the actuating signal $c_n(t)$ act as control inputs. Consequently, the on- and off-time control loops can be designed separately. For the on-time control loop, a PID controller, as reviewed in Section 2.2.4.1, can be used. Since a constant switching frequency is typically desired during steady state, the off-time loop should be active only during transient events to boost the converter’s performance. Thus, no steady state error compensation is required, and selecting a simpler compensator, e.g., a proportional (P) controller, is sufficient.

Hence, as soon as the models (2.86) and (2.87) are available, the controller design procedure for $T_{\text{on}}/T_{\text{off}}$ control does not differ from the design process for conventional duty cycle control.

Figure 2.18 reports an example of a $T_{\text{on}}/T_{\text{off}}$ control approach for the $n$th phase. While the voltage control loop acts on both the on-time and the off-time, current balancing is achieved by on-time regulation only.

### 2.2.4.3 FSF control

In contrast to the control schemes discussed previously, the design of the FSF controller is carried out in the time-domain utilizing the derived state-space model (2.73). In the following example, only the duty cycles are considered as control inputs. Of course, by starting from (2.86) instead of (2.73), an FSF $T_{\text{on}}/T_{\text{off}}$ controller can also be designed.
To achieve output voltage regulation to $V_{\text{ref}}$ and equal current sharing, (2.73) is first augmented by $N$ additional integrator states. While the first integrator removes any steady state error $\nu_{e,k}$ in the output voltage, the remaining $(N-1)$ ones ensure current balancing. The augmented system is therefore governed by

$$
\begin{pmatrix}
\ddot{x}_{iv,(k+1)} \\
\ddot{x}_{ic,(k+1)} \\
\ddot{x}_{k,(k+1)} \\
\ddot{x}_{FSF,(k+1)}
\end{pmatrix} =
\begin{pmatrix}
I & -c_1^T \\
0 & \Phi_{cb}
\end{pmatrix}
\begin{pmatrix}
\ddot{x}_{iv,k} \\
\ddot{x}_{ic,k} \\
\ddot{x}_{k} \\
\ddot{x}_{FSF,k}
\end{pmatrix}
+ \begin{pmatrix} 0 \\ H_{T_{sw}} \end{pmatrix} \ddot{d}_k.
$$

(2.88)

Here, $c_1^T$ denotes the first column of the output matrix $C$ and the system matrix of the current balancing integrators is defined as

$$
\Phi_{cb} :=
\begin{bmatrix}
0 & 1 & -1 & 0 & \cdots & 0 \\
0 & 0 & \ddots & \ddots & \vdots \\
\vdots & \ddots & \ddots & \ddots & 0 \\
0 & \cdots & 0 & 0 & 1 & -1
\end{bmatrix}
\in \mathbb{R}^{(N-1)\times(N+1)}.
$$

(2.89)
Hence, the updates of the integrator states $\dot{x}_{iv,(k+1)}$ and $\dot{x}_{ic,(k+1)}$ are computed as

$$\dot{x}_{iv,(k+1)} = \begin{bmatrix} 1 & 0 & \cdots & 0 \\ \end{bmatrix} x_{FSF,k}$$

$$= \dot{x}_{iv,k} - \tilde{v}_{out,k}, \quad (2.90)$$

and

$$\dot{x}_{ic,(k+1)} = \Phi_{cb} x_{FSF,k}$$

$$= \dot{x}_{ic,k} + \begin{bmatrix} \tilde{i}_{L_1,k} - \tilde{i}_{L_2,k} \\ \tilde{i}_{L_2,k} - \tilde{i}_{L_3,k} \\ \vdots \\ \tilde{i}_{L_{(N-1),k}} - \tilde{i}_{L_N,k} \\ \tilde{i}_{e,k} \end{bmatrix}, \quad (2.91)$$

respectively.

In the FSF controller, the input vector, i.e., the duty cycles, satisfies the equation

$$\dot{d}_k = -G_{FSF} x_{FSF,k}, \quad (2.92)$$

with the gain matrix $G_{FSF}$. Substituting the RHS of (2.92) for $\dot{d}_k$ in (2.88), yields the closed-loop system

$$\dot{x}_{FSF,(k+1)} = \Phi_{T_{sw,FSF}} x_{FSF,k} - H_{T_{sw,FSF}} G_{FSF} x_{FSF,k}$$

$$= \Phi_{T_{sw,FSF}} (\Phi_{T_{sw,FSF}} - H_{T_{sw,FSF}} G_{FSF}) x_{FSF,k}. \quad (2.93)$$

The required gain matrix $G_{FSF}$ for the desired closed-loop dynamics can be readily obtained by, e.g., pole placement [51] or linear-quadratic regulator (LQR) design.

The block diagram of the outlined FSF controller is presented in Figure 2.19. Note that, the thick arrows represent vectors. In contrast to the previously discussed PID and $T_{on}/T_{off}$ controllers, current balancing and voltage control are achieved by a single controller, which is furthermore common to all phases.

### 2.2.4.4 Comparison of the control schemes

In order to validate and compare the presented control approaches, a two-phase buck converter model has been used. The converter parameters are listed in Table 2.3.

Since the objective of the control schemes is to provide a specified output voltage even under varying operating conditions, load current variations have been applied to the converter. To allow for a fair comparison, all controllers have been designed according to similar
Figure 2.19: Example of an FSF controller for an N-phase converter.

Table 2.3: Two-phase buck converter parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$</td>
<td>3.3 V</td>
<td>$L_1, L_2$</td>
<td>3.3 µH</td>
</tr>
<tr>
<td>$C$</td>
<td>20 µF</td>
<td>$R_{p1}, R_{p2}$</td>
<td>220 mΩ</td>
</tr>
<tr>
<td>$R_{C}$</td>
<td>10 mΩ</td>
<td>$I_l$</td>
<td>0 A - 2 A</td>
</tr>
<tr>
<td>$V_{ref}$</td>
<td>1.25 V</td>
<td>$f_{sw}$</td>
<td>1.5625 MHz</td>
</tr>
<tr>
<td>$OS$</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2.4: Controller design parameters.

<table>
<thead>
<tr>
<th>Bandwidth</th>
<th>Value</th>
<th>Damping Factor</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_d, v_{out}$</td>
<td>55 kHz</td>
<td>$\zeta_d, v_{out}$</td>
<td>0.7</td>
</tr>
<tr>
<td>$f_{t_{off}, v_{out}}$</td>
<td>30 kHz</td>
<td>$\zeta_t, v_{out}$</td>
<td>1.0</td>
</tr>
<tr>
<td>$f_d, i_l$</td>
<td>40 kHz</td>
<td>$\zeta_d, i_l$</td>
<td>1.0</td>
</tr>
</tbody>
</table>
2.2 Switched-Mode Power Supplies

specifications. The design parameters, i.e., target closed-loop bandwidth and damping factor, are reported in Table 2.4. Note that, the $T_{on}/T_{off}$ control approach introduces the control of the off-time as an additional degree of freedom. Hence, the design parameters $f_{t_{off,v_{out}}}$ and $\xi_{t_{off,v_{out}}}$ apply to this scheme only. Since the on-time control loop in the $T_{on}/T_{off}$ approach should be dominant, a higher bandwidth $f_{t_{on,v_{out}}}$ than the off-time control loop bandwidth $f_{t_{off,v_{out}}}$ has been selected. Furthermore, the current balancing dynamics ($f_{d,i_{L}}$ and $f_{t_{on,i_{L}}}$) exhibit a lower bandwidth in comparison to that of the output voltage controls ($f_{d,v_{out}}$ and $f_{t_{on,v_{out}}}$), since removal of the steady state imbalance is sufficient. With all parameters available, the design of the PID and $T_{on}/T_{off}$ controllers has been carried out by a frequency compensation approach, whereas the required gain matrix $G_{FSF}$ of the FSF controller has been determined by pole placement.

In Figure 2.20, the simulated closed-loop responses of the three control schemes to a load drop from 2 A to 1 A followed by a load jump back to 2 A are reported. As can be seen, the PID and FSF controller achieve similar results with respect to the magnitude of the over- and undershoots as well as the settling time. This is expected, since the controllers have been designed according to the same specification. In contrast to that, the combined $T_{on}/T_{off}$ control approach clearly manages to reduce the over- and undershoots by appropriately increasing and decreasing the switching frequency.

Finally, in order to demonstrate the behavior of the current balancing control, the parasitic resistance $R_{p_{2}}$ of the second phase has been increased by 100 m$\Omega$. With the current balancing loop disabled, a mismatch between the phase currents $i_{L_{1}}(t)$ and $i_{L_{2}}(t)$ can be observed in Figure 2.21. As soon as the balancing loop is activated, $i_{L_{1}}(t)$ and $i_{L_{2}}(t)$ decrease and increase, respectively, until equal current sharing is attained. For the sake of brevity, only the transient response of the PID controller is depicted, which closely matches the response of the other schemes. Note that, the average values are depicted in Figure 2.21, since the current balancing aims to equalize the DC components of the phase currents.

The control laws discussed so far are all linear with respect to their control inputs. On the one hand, their design is relatively straightforward, utilizing the presented small-signal models and well-known linear control approaches. On the other hand, they disregard the fact that an SMPS is a VSS, i.e., a non-linear and time-variant system. Hence, large-signal stability can be hard to assess and the achievable dynamic performance may be unsatisfactory or dependent on the specific operating point. In order to overcome these shortcomings of linear control approaches, various non-linear control laws for SMPSs have been proposed in literature. These control laws typically consider the discontinuous nature and the switching behavior of an SMPS. One example of such a non-linear control law is SMC, which is especially
Figure 2.20: Load jump from 2 A to 1 A and back for a two-phase buck converter controlled by the three different control schemes.
suited for VSS. While analog SMC implementations for various SMPS types have been presented in literature, digital implementations are often impeded due to their limited resolution and bandwidth, resulting, e.g., in unsatisfactory accuracy. Before moving on to the main focus of this work, i.e., a digital SMC based control approach for multi-phase DC-DC converters, a brief general introduction to SMC is given in the next section.

2.3 SLIDING MODE CONTROL

In this section, the basic theory of SMC is reviewed, with special emphasis put on its application to SMPSs. The development of SMC control dates back to the 1960s, whereby the first internationally recognized works were published in 1976 [52], 1977 [53], and 1978 [54]. Since then, the research interest in this non-linear control law has been constantly increasing. In the context of power electronics, SMC first appeared as a promising control technique in the early 1990s, since its discontinuous control action is well suited for VSSs such as SMPSs [55]–[58]. Nevertheless, issues such as a potentially variable switching frequency often hamper the practical implementation of a sliding mode controller for SMPSs [19], [21], [59].

In contrast to many other control techniques, SMC applies a discontinuous control signal to the system. Hence, it switches from one continuous substructure in state space to another, representing a variable structure control method. As anticipated in Section 2.2.3, an SMPS consist of multiple substructures. The positions of the switches, controlled by discontinuous control inputs, determine the active configuration. This is furthermore highlighted by the set of state-space equa-

---

**Figure 2.21:** Inductor Currents $i_{L_1}(t)$ and $i_{L_2}(t)$ with mismatched phases after activation of the current balancing loop.
Fundamentals and State of the Art

Figure 2.22: Phase plane trajectories of the two possible configurations in a single-phase buck converter for different initial conditions.

The previously reviewed control techniques rely on small-signal models of the converter, which are operating point dependent in general. Unlike these control laws, SMC is based on the large-signal state-space representation of the SMPS. The control signals are directly calculated from the instantaneous state variables of the system such that the trajectory moves towards a region with a different subconfiguration in state space. To be more precise, the system trajectory is confined to a hyperplane in state space by the switching actions. This region is the so-called sliding surface defining the boundaries of the substructures at which the trajectory slides along until reaching equilibrium.

SMC can be divided into two phases. Firstly, an initial reaching phase, which steers the trajectory towards the sliding surface regardless of the initial conditions. Secondly, upon hitting the sliding surface, the state vector remains on it and slides towards the desired equilibrium. This phase is known as the sliding phase. Although the system switches between its different subconfigurations according to the discontinuous control inputs, the sliding surface is actually not part of the trajectories of any one subconfiguration. Consequently, the dynamics of a sliding mode controlled system are mainly gov-
2.3 Sliding Mode Control

The general form of an \( n \)th order VSS system, which is also valid for the multi-phase buck converter topology considered in this work, can be written as

\[
\dot{x}(t) = a(x(t), t) + B(x(t), t)c(x(t), t).
\]  

(2.94)

Here, \( x(t) \in \mathbb{R}^{n \times 1} \) defines the state vector, \( c(x(t), t) \in \mathbb{R}^{n \times 1} \) denotes the vector of discontinuous control inputs and \( t \) is the time variable. Furthermore, \( a(x(t), t) \in \mathbb{R}^{n \times 1} \) and \( B(x(t), t) \in \mathbb{R}^{n \times m} \) are vector-valued and matrix-valued functions, respectively, whereby \( a(x(t), t) \) and \( B(x(t), t) \) are assumed to be continuous. Since SMC represents a kind of state-feedback control, the vector of control inputs \( c(x(t), t) \) is a function of the system states. In contrast to the state vector (2.44), \( x(t) \) in (2.94) does not necessarily contain only the natural states of the system, e.g., the inductor currents \( i_L(t) \) and the capacitor voltage \( v_C(t) \). Rather, it is selected by the designer in order to represent the specified control objective such as output voltage regulation. The objective of the discontinuous control inputs \( c(x(t), t) \) is now to steer and then confine the state vector \( x(t) \) to the sliding surface \( \sigma(x(t)) = 0 \in \mathbb{R}^{n \times 1} \). Hence, the control action of the \( i \)th input \( c_i(x(t), t) \) can be simply expressed as [18]

\[
c_i(x(t), t) = \begin{cases} 
  c_{i}^{+}(x(t), t) & \text{if } \sigma_i(x(t), t) > 0 \\
  c_{i}^{-}(x(t), t) & \text{if } \sigma_i(x(t), t) < 0 
\end{cases}
\]  

(2.95)

In (2.95), \( c_{i}^{+}(x(t), t) \) and \( c_{i}^{-}(x(t), t) \) define the two possible states of the control input \( c_i(x(t), t) \). For an SMPS, those typically correspond to the on and off positions of an SPDT switch.

From (2.95), it directly follows that in order to calculate the control action and consequently achieve the desired control objective, a sliding surface has to be defined. The sliding surface has to be carefully chosen in such a way that the aforementioned reaching and sliding phases are entered, i.e., so called reaching and existence conditions have to be met. Furthermore, the stability of the system under sliding regime must be analyzed. In the next paragraphs, these three steps are outlined in a general fashion. For brevity, the time dependency of the state vector \( x(t) \) and the input vector \( c(x(t), t) \) are omitted for the remainder of this section.

2.3.1 Existence Conditions

During sliding mode operation, the system trajectory moves along the defined surface \( \sigma(x) = 0 \). A sufficient condition for the existence
of such a sliding motion can be derived based on Lyapunov’s second method. To that end, the Lyapunov function candidate
\[ V(\sigma(x)) = \frac{1}{2} \sigma^T(x) \sigma(x) \]
in considered. If the condition
\[ \frac{dV(\sigma(x))}{dt} = \frac{\partial V(\sigma(x))}{\partial \sigma(x)} \frac{d\sigma(x)}{dt} = \sigma^T(x) \dot{\sigma}(x) < 0 \]
is verified in a neighborhood of \( \sigma(x) = 0 \), a sliding motion indeed exists.

2.3.2 Reaching conditions

In addition to the existence of a sliding mode, it is also necessary to verify that the hypersurface \( \sigma(x) = 0 \) is actually reached from a given state vector \( x \). If the state vector belongs to the subspace \( \{ x \in \mathbb{R}^n \mid \sigma^T(x) \dot{\sigma}(x) < 0 \} \), this is ensured since \( \sigma^T(x) \dot{\sigma}(x) < 0 \) implies that the trajectory moves towards \( \sigma(x) = 0 \). As a consequence, all possible initial conditions have to come from (2.98) in order to fulfill the reaching conditions.

2.3.3 Stability

Even if the above two conditions are fulfilled, no statements about the stability of the sliding mode can be made. Thus, it is furthermore necessary to assess the actual dynamics of the sliding mode operation. A description of the system during the sliding phase can be obtained by applying the equivalent control principle. As already mentioned, under SMC, the trajectory remains on the sliding surface and hence
\[ \sigma(x) = 0 \]
also holds, which can be expressed as
\[ \dot{\sigma}(x) = \frac{\partial \sigma(x)}{\partial x} \dot{x} = \frac{\partial \sigma(x)}{\partial x} \left( a(x,t) + B(x,t) c(x) \right) = 0. \]
Then, by solving (2.100) for \( c(x) \) one obtains the equivalent continuous control
\[ c_{eq}(x) := -\left( \frac{\partial \sigma(x)}{\partial x} B(x,t) \right)^{-1} \frac{\partial \sigma(x)}{\partial x} a(x,t). \]
From (2.101), it follows that \( \left( \frac{\partial \sigma(x)}{\partial x} B(x,t) \right)^{-1} \) has to be full rank. In other words, a control action that moves the trajectory towards the
sliding surface must always exist. It is important to stress that, the control vector \( c_{\text{eq}} (x) \) is not actually applied to the system. Rather, the high frequency switching of the control inputs that forces the state vector \( x \) onto the sliding surface \( \sigma (x) = 0 \) behaves like this continuous control \( c_{\text{eq}} (x) \).

Finally, by substituting \( c (x (t), t) \) in (2.94) with the RHS of (2.101), the dynamics of the system under sliding regime are readily obtained as

\[
\dot{x} = a(x, t) + B(x, t) c_{\text{eq}}(x) = a(x, t) \left( I - B(x, t) \left( \frac{\partial \sigma(x)}{\partial x} B(x, t) \right)^{-1} \frac{\partial \sigma(x)}{\partial x} \right). \tag{2.102}
\]

Since (2.102) is non-linear in general, stability has to be assessed by, e.g., Lyapunov’s methods. As will be shown later, under sliding regime, the proposed SMC law for the multi-phase buck converter yields an LTI system. Hence, investigation of the system matrix, i.e., the location of its eigenvalues, is sufficient in order to analyze stability.

As a consequence of the sliding motion, the closed-loop system, given by (2.102), is of lower order than the original system (2.94). To be more precise, (2.102) is of order \((n - m)\). This order reduction property is one of the key benefits of SMC.

### 2.3.4 Application to switched-mode power supplies

With the fundamentals of SMC as set out above, a controller for a buck converter is designed in the following. Proceeding from the schematic of an ideal \( N \)-phase converter depicted in Figure 2.5, the state-space model

\[
\dot{x} = a(x) + b c(x) \tag{2.103}
\]

can be derived. As already anticipated, the state vector does not necessarily correspond to the natural states of the plant. In this example,

\[
x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} v_{\text{out}} - V_{\text{ref}} \\ \frac{d(v_{\text{out}} - V_{\text{ref}})}{dt} \end{bmatrix} = \begin{bmatrix} v_{\text{out}} - V_{\text{ref}} \\ \frac{i_{\text{C}}}{L} \end{bmatrix} \tag{2.104}
\]

is selected, since the objective is to regulate \( v_{\text{out}} \) to the desired value \( V_{\text{ref}} \) and keep it constant. For the state vector as specified in (2.104), \( a(x) \) and \( b \) are readily obtained as

\[
a(x) = \begin{bmatrix} x_2 \\ -\frac{N(x_1 + V_{\text{ref}})}{L} \end{bmatrix}, \tag{2.105}
\]

and

\[
b = \begin{bmatrix} 0 \\ \frac{N V_{\text{in}}}{L} \end{bmatrix}, \tag{2.106}
\]
respectively. Note that, the load current, which can be considered as a disturbance to the system, is neglected in this simple example. Furthermore, only a single control input, which is simultaneously applied to all SPDT switches, is present in this case. Consequently, $b$ reduces to a vector-valued function. Recalling that the SPDT switches can only assume two distinct states, the possible control inputs are defined as $c^+ (x) := 0$ and $c^- (x) := 1$. This directly follows from the consideration that the SPDT switches have to be closed (opened) if $(v_{out} - V_{ref})$ is negative (positive) in order to move the state vector towards the origin.

Next, a linear combination of the states, i.e.,

$$\sigma (x) = \begin{bmatrix} 1 \\ \tau \end{bmatrix} x = 0,$$  \hspace{1cm} \text{(2.107)}

is chosen as the sliding surface. Here, $\tau$ represents a yet to be defined design parameter, which essentially influences the closed-loop dynamics of the system under SMC.

For the selected sliding surface definition (2.107), its derivative calculates to

$$\dot{\sigma} (x) = \frac{\partial \sigma (x)}{\partial x} \dot{x} = \frac{\partial g x}{\partial x} \dot{x} = \begin{bmatrix} 1 & \tau \end{bmatrix} \dot{x} = \dot{x}_1 + \tau \dot{x}_2,$$ \hspace{1cm} \text{(2.108)}

which yields the existence condition

$$\sigma (x) \dot{\sigma} (x) = (x_1 + \tau x_2) (\dot{x}_1 + \tau \dot{x}_2) < 0.$$ \hspace{1cm} \text{(2.109)}

Substituting $\dot{x}_1$ and $\dot{x}_2$ in (2.109) with the RHS of (2.103) and expanding the terms yields the more vivid representation

$$r_1 (x) := x_2 + \frac{\tau N}{L C} (V_{in} - x_1 - V_{ref}) > 0 \quad \text{if} \quad \sigma (x) < 0 \hspace{1cm} \text{(2.110a)}$$

$$r_2 (x) := x_2 - \frac{\tau N}{L C} (x_1 + V_{ref}) < 0 \quad \text{if} \quad \sigma (x) > 0.$$ \hspace{1cm} \text{(2.110b)}

Note that, the lines $r_1 (x) = 0$ and $r_2 (x) = 0$ define the boundaries of the existence region in the phase plane. In other words, if the sliding surface $\sigma (x) = 0$ is hit while (2.110) is fulfilled, sliding mode operation is entered. Furthermore, by solving (2.110) for $\tau$, the constraints on the slope of the sliding surface can be readily obtained.

Moreover, reaching conditions have to be fulfilled. For the second-order system (2.103) with the sliding surface defined as in (2.107), it is straightforward to check whether the existence conditions are met or not. In fact, if the equilibrium points of the state vector $x$ with $c (x) = c^+ (x) = 0$ and $c (x) = c^- (x) = 1$ fulfill the conditions
\( \sigma(X^+) < 0 \) and \( \sigma(X^-) > 0 \), respectively, it is guaranteed that the sliding surface is reached. By solving

\[
\dot{x} = a(x) + bc(x) = \begin{bmatrix} x_2 \\
\frac{N(cV_{in} - x_1 - V_{ref})}{LC} \end{bmatrix} = \begin{bmatrix} 0 \\
0 \end{bmatrix}
\] (2.111)

for \( x \), one obtains the equilibrium points

\[
X^\pm = \begin{bmatrix} 0 \\
c(x) V_{in} - V_{ref} \end{bmatrix}
\] (2.112)

for the binary input \( c(x) \). Hence, from (2.112) it follows that the reaching conditions

\[
\sigma(X^+) = gX^+ = -\tau V_{ref} < 0 \] (2.113a)

\[
\sigma(X^-) = gX^- = -\tau (V_{in} - V_{ref}) > 0 \] (2.113b)

are verified if \( \tau > 0 \).

In addition to the considerations above and the restriction imposed by (2.110) on \( \tau \), stability of the sliding mode has to be assessed. To that end, following the equivalent control approach outlined in Section 2.3.3, a first order LTI system description of the sliding mode controlled converter is obtained. First, \( c_{eq}(x) \) is calculated according to (2.101), yielding

\[
c_{eq}(x) = -\left( \begin{bmatrix} 1 & \tau \\
\frac{NV_{in}}{LC} \end{bmatrix} \right)^{-1} \begin{bmatrix} 1 \\
\frac{x_2}{N(x_1 + V_{ref})} \end{bmatrix}
\] (2.114)

Then, by substituting \( c \) in (2.103) with the RHS of (2.114), the autonomous system

\[
\dot{x} = a(x) + bc_{eq}(x) = \begin{bmatrix} x_2 \\
\frac{N(x_1 + V_{ref})}{LC} \end{bmatrix} + \begin{bmatrix} 0 \\
0 - \frac{x_2}{\tau} \end{bmatrix}
\] (2.115)

which describes the dynamics under sliding regime, is obtained. Due to the order reduction property of SMC, one eigenvalue of (2.115) is located at zero. Moreover, in order to guarantee a stable sliding mode, the second eigenvalue, located at \( -\frac{1}{\tau} \), has to lie in the left half-plane. Hence, \( \tau \) has to be strictly positive for the stability condition to be
fulfilled. To conclude, under sliding regime, the converter behaves like a first order system with time constant $\tau$. Hence, the relationship between the time constant $\tau$ and the closed-loop bandwidth $f_{eq}$ is given by

$$\tau = \frac{1}{2\pi f_{eq}}. \quad (2.116)$$

As (2.115) implies, the dynamics of the sliding motion are fully defined by the sliding surface $\sigma(x)$ and thus independent of the number of phases $N$ and circuit parameters such as the values of $L$ and $C$. Nevertheless, the boundaries of the existence region depend on the actual system. Furthermore, during the reaching phase, the trajectory of the state vector $x$ is defined by the dynamics of the active sub-configuration. Hence, during transient events, such as the converter’s start-up or a load change, the initial trajectory depends on the system parameters. Only upon hitting the sliding surface, the dynamics are governed by (2.115). This further highlights the importance of the existence region bounded by (2.110).

In order to demonstrate the behavior of a sliding mode controlled SMPS, simulations for a two-phase buck converter have been carried out. As for the linear control schemes presented in Section 2.2.4, the parameters of the converter have been selected as reported in Table 2.3. In contrast to the DT controllers discussed in Section 2.2.4, the SMC law presented here is implemented in CT. Thus, (2.107) is evaluated with the CT state vector as given in (2.104). Figure 2.23 reports the output voltage responses to a changing step load, varying between 2 A and 1 A. Two different values of $\tau$, namely, $\tau_1$ and $\tau_2$, yielding the closed-loop bandwidths $f_{eq,1} = 55$ kHz and $f_{eq,2} = 110$ kHz, respectively, are compared to each other. As anticipated, the value of $\tau$ determines the speed of the dynamic response. Furthermore, as illustrated by the phase trajectories in Figure 2.24, a larger bandwidth causes a reduced existence region. Hence, the choice of $\tau$ implies a tradeoff between dynamic performance and stability.

### 2.3.5 Practical implementation issues

As outlined, SMC allows for a straightforward controller design while achieving an excellent dynamic performance. Nevertheless, in order to successfully apply SMC to SMPSs, various practical implementation issues need to be addressed.

One of the most critical problems is the switching frequency. The previously presented linear control schemes guarantee a constant frequency (with the exception of $T_{on}/T_{off}$ control during transients). In contrast to that, the control action of SMC is given by (2.95), which implies that the control signal immediately changes if the sliding surface is crossed. In theory, this can result in an infinitely high switching frequency (2.96). However, in practice, the switching frequency is limited by the switching frequency of the semiconductor devices used. This limits the achievable bandwidth of the converter and thus affects its performance.
Figure 2.23: Load jump from 2 A to 1 A and back for a two-phase buck converter under SMC. Two different values of $\tau$ are compared to each other.
Figure 2.24: Phase plane trajectory of the sliding mode controlled converter’s state vector $x(t)$ during a typical transition from start-up to steady state followed by the load changes depicted in Figure 2.23b.
frequency. Of course, in practice, the switching frequency has to be limited. To that end, various solutions have been investigated in literature. For SMPSs, hysteresis SMC [28], [42], [60], implementation of the equivalent control command $c_{eq}$ [24], and synchronization with a set-reset (SR) flip-flop [25], [26] have been successfully employed. Although a constant switching frequency can be easily achieved by the latter two methods, benefits of SMC, such as its robustness and disturbance rejection, might be lost. In hysteresis SMC, a hysteresis window of width $2h$ is added to the comparator generating the control signals, i.e., (2.95) is replaced by

$$
c_i(x(t),t) = \begin{cases} 
c_i^+(x(t),t) & \text{if } \sigma_i(x(t),t) > h \\
c_i^-(x(t),t) & \text{if } \sigma_i(x(t),t) < -h 
\end{cases} \quad (2.117)
$$

While introducing such a hysteresis window limits the switching frequency, it still depends on the operating point. Therefore, various dynamic hysteresis SMC concepts have been proposed to obtain a constant switching frequency [24], [59]. In order to adapt to changes in the operating conditions, the hysteresis width of the comparator is dynamically adjusted based on, e.g., the input voltage or the switching frequency error. While the first method allows for a simpler implementation, the second one achieves tighter regulation, since it better adapts to parameter variations.

Another issue of SMC arises from the information required to calculate the sliding surface. Similar to the FSF control reviewed in Section 2.2.4.3, SMC relies on knowledge of the whole state vector. Thus, current sensing is typically required [24]. Since the phase currents have to be sampled at a high rate, the implementation effort for a digital controller is significantly increased. In order to overcome this issue, different current observers have been proposed in literature [15], [26], [61], [62]. With these observers, the phase currents are digitally reconstructed, which can reduce the hardware complexity dramatically.

Finally, in interleaved multi-phase converters a delay of $\frac{T_{sw}}{N}$ between the control signals $c_{1,2,\ldots,N}$ of the individual phases is required. Consequences of this phase shift are the desired properties of ripple reduction and effective switching frequency increase. By means of shifting the PWM ramps, a proper phase shift is easily achieved in linear control schemes [63]. Similarly, obtaining the required phase shift in SR flip-flop SMC or equivalent control SMC is straightforward. Delaying the external trigger signals [61], [64] or the ramp signals [65], respectively, is sufficient. However, implementations with a hysteresis band typically define one of the phases as a master phase and the phase shift is obtained by the selection of the slaves’ switching functions [28], [42], [59], [66], [67]. Therefore, the master phase has to be always operational. Another major drawback of this kind of implementation is the dependency of interleaved operation on converter
parameters. For a multi-phase buck converter it has been shown that the conditions [66]

\[ D < 0.5 \Rightarrow D > \frac{1}{N} \]  

(2.118a)

\[ D > 0.5 \Rightarrow D < 1 - \frac{1}{N} \]  

(2.118b)

with the steady state duty cycle \( D \) as defined in (2.30), have to hold in order to accomplish and maintain the proper phase shift. Therefore, specification parameters such as the input voltage \( V_{in} \) and the desired output voltage \( V_{ref} \) define the number of required phases for interleaved operation. It can be easily shown that it is not possible to operate an interleaved two-phase buck converter with the aforementioned method, since the constraints in (2.118) would never be fulfilled. Hence, a solution which is not limited by the constraints (2.118) is required in order to successfully employ hysteresis SMC for interleaved converters.

In this section, the basic principle of SMC and its suitability for SMPSs has been reviewed. Furthermore, the most important implementation issues, which are addressed in this work, have been highlighted. As already outlined, SMC exhibits a high robustness with respect to parameter variations. Nevertheless, in practice, due to various aspects, such as the desired constant switching frequency operation and different configurations that have to be supported by a single controller for the SMPS, the actual achievable performance and robustness of SMC might be reduced. Therefore, it is beneficial to have an accurate system description, e.g., a state-space model, available in order to tune the controller accordingly. One way to obtain such a model of the actual system is by the means of SI. Thus, in the next section, an overview of state-of-the-art LLS SI approaches and their application to SMPSs is given.

2.4 SYSTEM IDENTIFICATION

As already outlined in the previous sections, today’s electronic devices require highly efficient, accurate, and reliable SMPSs. An insufficiently performing SMPS might have a negative impact on the system’s operating range, stability and reliability. In order to provide a well-regulated output voltage under all operating conditions, the use of sophisticated control concepts is essential [14], [15]. Manufacturing tolerances, temperature dependency and long-term aging effects can degrade the performance of an SMPS [68]. Adaptive schemes have been proposed to improve the performance of model predictive control in the presence of parameter mismatches between the model and the actual system [68], [69]. In other control approaches, controller
coefficients often have to be conservatively chosen, in order to cover worst case parameter spreads or different sets of passive components. This can lead to an unsatisfactory performance [70], [71]. By employing online SI, the actual converter parameters can be estimated [35], [72]–[77]. Subsequently, these estimates may be used in order to auto-
tune the controller, yielding improved stability and dynamic perfor-
ance [71], [75], [76], [78].

SI can be divided into two main approaches: non-parametric and parametric ones [79]. In non-parametric SI, a fixed system model is not required. Typical examples of non-parametric SI methods applicable for controller tuning are approaches that apply correlation analysis and Fourier transform methods to obtain the frequency response of the system. A downside of these approaches are their relatively high computational complexity and the long stimulus injection time [32], [34], [78]. Moreover, the controller tuning is then usually limited to frequency response methods [71]. On the one hand, a fixed system model, which introduces additional uncertainties, is assumed in parametric SI. On the other hand, the computational complexity is usually reduced in comparison to Fourier transform methods [72], [73], [75], [76]. Another benefit is that the controller tuning is simplified, since the identification result, e.g., a DT TF model of the system, can be directly used for the tuning process [33], [80].

In contrast to the aforementioned SI techniques, which are not exclusive to the field of SMPSs, DC-DC converter specific approaches also exist. In [40], [81], SI methods based on limit cycle oscillations have been investigated. In these approaches, a relay element is intro-
duced in the feedback loop, which causes a limit cycle oscillation of the output voltage. The amplitude and frequency of this oscillation contains information about the converter, which is subsequently used for controller tuning. Although these methods can be implemented with very low computational complexity, they typically suffer from larger perturbation amplitudes and a lower accuracy than other SI approaches [47].

A model reference-based tuning approach has been proposed in [82], which combines the SI and tuning into a single step. This method achieves a high tuning accuracy, while requiring few computational complex operations. Nevertheless, since the controller coefficients are continuously adapted until the tuning objective is achieved, this might lead to instabilities.

In typical parametric SI approaches for SMPSs, a stimulus, such as a pseudorandom binary sequence (PRBS) or a chirp signal, is super-
imposed on the steady state duty cycle [72], [73]. Then, the stimu-
lus and the measured output voltage perturbation are used to esti-
mate the coefficients of a DT TF model of the converter. Various es-
[83], the iterative LLS (ILS) algorithm, which requires a large number of multiplications, is employed for estimation. A computationally less complex SI approach has been presented in [71]. Therein, the exponentially weighted recursive least squares (ERLS) with dichotomous coordinate descent (ERLS-DCD) algorithm [84] is employed for estimating the TF parameters. Later, this approach has been extended to estimate the TFs of multi-rail converters and subsequently tune the controller of each individual converter [85]. A self-tuned Kalman filter approach has been proposed in [73]. While this approach can improve the convergence speed and estimation accuracy especially in the presence of abrupt load changes, the computational complexity is increased in comparison to the ERLS-DCD algorithm. Due to their long stimulus injection times and high computational complexities, these approaches contradict the usual low power and small area requirements.

In [72], a concept using the step-adaptive approximate LLS (ALS) (SALS) estimator [86], an algorithm similar to the Randomized Kaczmarz algorithm [87], has been proposed. In contrast to previously presented SI approaches, the method suggested therein can operate at higher switching frequencies and is computationally less complex. Nevertheless, in [72], only an accurate estimate of the converter’s natural frequency is obtained and no controller auto-tuning is performed.

### 2.4.1 Linear least squares estimation

An exemplary system model for a parametric SI approach is illustrated in Figure 2.25. Here, a system model $\hat{g}_k$, e.g., a finite impulse response (FIR) filter, is first selected. Then, the parameters of the model are derived such that some cost function, e.g., of the estimation error $e_k$, is minimized. As many other parametric SI approaches for SMPSs, this work focuses on LLS estimation, which assumes a linear model for $\hat{g}_k$, and the objective is to minimize the sum of squared errors. In the following, the fundamental principle of LLS estimation is reviewed in more detail.
Choosing an FIR filter with \( P \) taps as the linear model, the relationship between the output of the system and its input can be written in linear form as
\[
y = H\theta + n. \tag{2.119}
\]
In (2.119), the output vector is given as
\[
y = \begin{bmatrix}
y_0 \\
y_1 \\
\vdots \\
y_M
\end{bmatrix} \in \mathbb{R}^{M \times 1}, \tag{2.120}
\]
the observation matrix as
\[
H = \begin{bmatrix}
x_0 & 0 & \cdots & 0 \\
x_1 & x_0 & \cdots & 0 \\
\vdots & \vdots & \ddots & \vdots \\
x_{(M-1)} & x_{(M-2)} & \cdots & x_{(M-P)}
\end{bmatrix} \in \mathbb{R}^{M \times P}, \tag{2.121}
\]
the parameter vector, which contains the coefficients of the FIR filter, as
\[
\theta := \begin{bmatrix}
b_{(P-1)} \\
b_{(P-2)} \\
\vdots \\
b_0
\end{bmatrix} \in \mathbb{R}^{P \times 1}, \tag{2.122}
\]
and the measurement noise is considered by the vector \( n \). The number of measurements is determined to be \( M \). Although an FIR filter model is assumed in this introductory example, this approach is also easily applicable for models with an infinite impulse response (IIR), as shown in Section 2.4.2. Observe that, (2.119) has no exact solution in general, since typically \( M > P \), i.e., the system of equations is overdetermined, and the measurements are furthermore corrupted by noise and model inaccuracies may exist. Instead, the LLS solution of (2.119) is obtained by minimizing the cost function
\[
J(\theta) = (y - H\theta)^T (y - H\theta), \tag{2.123}
\]
i.e.,
\[
\hat{\theta} = \arg\min_{\theta \in \mathbb{R}^{P \times 1}} J(\theta). \tag{2.124}
\]
In other words, the minimization of (2.123) yields the parameter vector estimate \( \hat{\theta} \) comprising the estimates of the filter coefficients. Although the analytical solution to (2.123) can be calculated as
\[
\hat{\theta} = \left( H^T H \right)^{-1} H^T y, \tag{2.125}
\]
the involved multiplications and matrix inversion pose a significant challenge for many applications due to their high computational complexity and numerical precision requirements. A more detailed discussion on practical implementation issues follows in Section 2.4.3.

### 2.4.2 Application to switched-mode power supplies

With the fundamentals of LLS SI reviewed, its application to SMPSs is outlined in the example of a single-phase buck converter in this section. The converter parameters are reported in Table 2.5. In this example, the objective is to identify the small-signal dynamics of the plant. To be more precise, an estimate \( \hat{G}_{d,v_{\text{out}}} (z) \) of the DT duty-cycle-to-output-voltage TF \( G_{d,v_{\text{out}}} (z) \) shall be obtained. For the converter model derived in Section 2.2.3, it can be shown that \( G_{d,v_{\text{out}}} (z) \) represents a second-order IIR filter of the form

\[
G_{d,v_{\text{out}}} (z) = \frac{V_{\text{out}} (z)}{D (z)} = \frac{b_1 z + b_0}{z^2 + a_1 z + a_0},
\]

which is fully described by the coefficient vector

\[
\theta := \begin{bmatrix} a_1 \\ a_0 \\ b_1 \\ b_0 \end{bmatrix}.
\]

Thus, the SI process boils down to calculating an estimate \( \hat{\theta} \) of \( \theta \).

In the DT domain, the relationship between the duty cycle \( d_k \) and the output voltage \( v_{\text{out},k} \) in the \( k \)th switching period can be written as

\[
v_{\text{out},k} = -a_1 v_{\text{out},(k-1)} - a_0 v_{\text{out},(k-2)} + b_1 d_{(k-1)} + b_2 d_{(k-2)}. \tag{2.128}
\]

For SI purposes, the input should be excited by a frequency rich noise signal. Therefore, the duty cycle \( d_{c,k} \), which is in this example calculated by a PID controller, is superimposed by the PRBS \( d_{p,k} \) with a peak-to-peak amplitude of 0.1 and a duration of \( M = 511 \) switching cycles. The duty cycle \( d_k = d_{c,k} + d_{p,k} \) and the sampled output voltage

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{in}} )</td>
<td>3.3 V</td>
<td>( L )</td>
<td>3.3 µH</td>
</tr>
<tr>
<td>( C )</td>
<td>20 µF</td>
<td>( R_p )</td>
<td>220 mΩ</td>
</tr>
<tr>
<td>( R_C )</td>
<td>10 mΩ</td>
<td>( I_l )</td>
<td>0 A - 2 A</td>
</tr>
<tr>
<td>( V_{\text{ref}} )</td>
<td>1.25 V</td>
<td>( f_{\text{sw}} )</td>
<td>1.5625 MHz</td>
</tr>
<tr>
<td>( OS )</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
During stimulus injection are shown in Figure 2.26. It is worth noting that, a large-signal VSS model of the single-phase converter has been used to obtain the waveforms reported in Figure 2.26.

From (2.128), it follows that the relation between the duty cycle and the output voltage during injection of the perturbation can be conveniently written in matrix form as

\[ v_{\text{out}} = H \theta. \]  

(2.129)

Here,

\[ v_{\text{out}} = \begin{bmatrix} v_{\text{out},0} \\ v_{\text{out},1} \\ \vdots \\ v_{\text{out},(M-1)} \end{bmatrix} \]  

contains the output voltage samples of \( M \) switching periods, and the observation matrix is given as

\[ H = \begin{bmatrix} 0 & \cdots & \cdots & 0 \\ -v_{\text{out},0} & 0 & d_0 & 0 \\ -v_{\text{out},1} & -v_{\text{out},0} & d_1 & d_0 \\ \vdots & \vdots & \vdots & \vdots \\ -v_{\text{out},(M-2)} & -v_{\text{out},(M-3)} & d_{(M-2)} & d_{(M-3)} \end{bmatrix}. \]  

(2.131)

In contrast to the more general case outlined in Section 2.4.1, a noiseless measurement of \( v_{\text{out},k} \) is assumed. Also note that, the 0th switching period, i.e., \( v_{\text{out},0} \) and \( d_0 \) marks the start of the stimulus injection.

After the stimulus injection has finished, \( \hat{\theta} \) is calculated according to (2.125). A comparison between the frequency responses of the analytical TF \( G_{d,v_{\text{out}}}(z) \), which can be obtained by (2.74), and its SI estimate \( \hat{G}_{d,v_{\text{out}}}(z) \) is shown in Figure 2.27. As can be seen, in this simple example without measurement noise, the identified model matches the derived TF very closely. In the next section, some implementation aspects that have to be considered, e.g., computational complexity, estimation accuracy, finite precision, measurement noise and quantization effects are discussed.

### 2.4.3 Practical implementation issues

Typically, it is desired to implement the digital control part of an SMPS with a small footprint in terms of power consumption and area. Therefore, computationally complex operations, bit widths, memory and computation time should be reduced to a minimum. Of course, these aspects also have to be considered during the design process of an SI concept, since such a feature increases the amount of required digital hardware. Therefore, low complexity SI schemes are necessary.
Fundamentals and State of the Art

Figure 2.26: Exemplary waveforms of the duty cycle $d_k$ and the output voltage $v_{\text{out},k}$ during SI.

(a) Applied duty cycle $d_k$ composed of the duty cycle $d_{c,k}$, as calculated by the controller, and the perturbation $d_{p,k}$, which is injected for SI purposes.

(b) Perturbed output voltage caused by the injection of the SI stimulus $d_{p,k}$. 

\begin{figure}[h]
\centering
\includegraphics[width=0.8\textwidth]{figure.png}
\caption{Exemplary waveforms of the duty cycle $d_k$ and the output voltage $v_{\text{out},k}$ during SI.}
\end{figure}
As already anticipated, directly calculating (2.125) is not feasible in many digital hardware implementations. The main disadvantages of this so called batch LLS (BLS) estimator are its large memory requirements, the high computational complexity, e.g., the number of required multiplications and the high numerical precision needed. Hence, various algorithms to approximate the exact solution (2.125) of the LLS minimization problem have been proposed. One common approach is the ILS algorithm, which uses the gradient descent technique [88]. In contrast to BLS, the ILS algorithm solves the LLS problem in an iterative manner. Despite its widespread use, the ILS algorithm suffers from poor accuracy for fixed point implementations with low bit widths and the relatively large number of required multiplications [89]. In the context of SMPSs, the ERLS-DCD [84] algorithm has been successfully employed for SI purposes [35], [85]. On the one hand, the number of required multiplications is significantly reduced by the ERLS-DCD algorithm in comparison to other algorithms such as ILS. On the other hand, its different configuration parameters make this algorithm hard to tune. In Table 2.6, the computational complexity of BLS, ILS and ERLS-DCD in terms of required multiplications is compared. The number of iterations is denoted by $I$. Note that, the BLS obtains the solution in one iteration, whereas $I \geq M$ holds for the other estimators.

Next to the computational complexity, other properties of an LLS approximation algorithm have to be considered in order to assess its performance. Two properties which are of special interest if the SI result is to be used for controller tuning are the estimation accuracy
Table 2.6: Comparison of the required number of multiplications.

<table>
<thead>
<tr>
<th>Method</th>
<th>Multiplications</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLS</td>
<td>$\frac{1}{6}p^3 + P^2M + PM$</td>
</tr>
<tr>
<td>ILS</td>
<td>$I(2PM + P)$</td>
</tr>
<tr>
<td>ERLS-DCD</td>
<td>$I(2P^2 + 3P)$</td>
</tr>
</tbody>
</table>

and convergence speed. If the estimation accuracy is low, i.e., $\hat{g}_k$ does not describe $g_k$ well, the controller might be inadequately tuned. This in turn can degrade the dynamic performance or, in the worst case, even result in instability. Although estimation accuracy can often be improved by increasing the number of iterations $I$, or the length $M$ of the stimulus, or both, this increases calculation time and complexity. Therefore, convergence speed is another important parameter.

In addition, the amplitude of $d_{p,k}$ has to be carefully chosen. Greater magnitudes of $d_{p,k}$ typically improve the estimation accuracy and convergence speed, while simultaneously increasing the perturbation on the output voltage and inductor currents. Hence, the amplitude choice depends on various parameters such as tolerable output voltage deviation, noise level, and ADC resolution. Similar to the amplitude of $d_{p,k}$, the stimulus injection time constitutes a design parameter. On the one hand, longer injection times usually improve the estimation accuracy. On the other hand, the number of rows of the observation matrix $H$ is determined to be $M$, hence, more multiplications are required.

Another issue of SI concepts for SMPSs is their applicability to sophisticated control concepts. Despite the strong research interest in SI, typically only converters operated with voltage mode controllers, e.g., the ones reviewed in Section 2.2.4, are considered when investigating identification and auto-tuning methods. In contrast to that, the increasing amount of required features in today’s electronic devices has fostered the popularity of control concepts offering an improved performance, such as SMC. As discussed in Section 2.3, in these control schemes, the controller usually does not calculate a duty cycle. Instead, the states of the power switches are directly controlled. As a consequence, perturbing the duty cycle is not easily possible, and only considering the TFs $G_{d_{p,v_{out}}}(z)$ is not sufficient for controller tuning. Therefore, different approaches enabling SI and controller auto-tuning for these kind of control laws have to be investigated.
In this chapter, an innovative digital sliding mode controller for interleaved multi-phase buck converters is presented. A dynamic hysteresis band for constant switching frequency operation is used. By utilizing the proposed multi-dimensional sliding surface approach, a straightforward controller design, including current balancing for an arbitrary number of phases is achieved. In contrast to state-of-the-art methods, the phases operate masterless, thus, individual control commands and hysteresis widths are calculated for each phase. Moreover, a novel concept for obtaining the desired phase shift for interleaved operation is suggested, even for specifications not fulfilling constraint (2.118). Hence, unlike state-of-the-art implementations, the proposed solution does not limit the obtainable output voltage range dependent on the number of interleaved phases. The presented method dynamically adjusts the hysteresis window based on the phase shift error in order to achieve the desired interleaving operation. Additionally, analytical \( DT \) small-signal models of the proposed phase shift and frequency control loops are derived for the first time. The analytical models are then validated by means of simulation. Although simulation results are provided for a two-phase buck converter, the approach is also applicable to converters with more phases and other topologies.

### 3.1 Converter Model

For convenience, although already introduced in Section 2.2.2, the schematic of a typical \( N \)-phase synchronous buck converter is depicted again in Figure 3.1. Here, a simplified version of an SMC loop is also depicted in the figure. In contrast to PWM based controllers, the actuating signals \( c_{1,2,...,N} \) are generated by the highlighted comparators. Exemplary input and output waveforms of the employed comparators with a hysteresis window of width \( 2h_n \) are reported in Figure 3.2.

As anticipated in Section 2.3.4, the converter illustrated in Figure 3.1 can be modeled by a \( VSS \) system of order \( (N+1) \) governed by

\[
\dot{x}(t) = Ax(t) + Bc(t),
\]

with the system matrix denoted as \( A \in \mathbb{R}^{(N+1) \times (N+1)} \), and the input matrix given as \( B \in \mathbb{R}^{(N+1) \times N} \). In (3.1),

\[
x(t) = \begin{bmatrix} v_{\text{out}}(t) & i_{L_1}(t) & \ldots & i_{L_N}(t) \end{bmatrix}^T \in \mathbb{R}^{(N+1) \times 1},
\]
Figure 3.1: Schematic of an $N$-phase synchronous buck converter. A simplified version of an SMC loop, including the comparators with hysteresis, is also illustrated.

Figure 3.2: Exemplary input and output waveforms of the employed comparators with hysteresis.
and
\[
c(t) = \left[ c_1(t) \ldots c_N(t) \right]^T \in \{0, v_{\text{in}}(t)\}^{N \times 1}
\]
\[ (3.3) \]
denote the state and input vector, respectively. By applying KVL and KCL to the system in Fig. 3.1 the matrices
\[
A = \begin{bmatrix}
-\frac{Y_o}{C} - Z_t & -\frac{1}{L_1} & \ldots & -\frac{1}{L_N} \\
\frac{Y_o}{C} - \frac{Y_o R C R_p}{L_1} & -\frac{R_p}{L_1} & 0 & \ldots \\
\vdots & 0 & \ddots & 0 \\
\frac{Y_o}{C} - \frac{Y_o R C R_p N}{L_N} & 0 & \ldots & -\frac{R_p N}{L_N}
\end{bmatrix}
\]
\[ (3.4) \]
and
\[
B = \begin{bmatrix}
\frac{R_l Y_o}{L_1} & \ldots & \frac{R_l Y_o}{L_N} \\
\frac{1}{L_1} & 0 & \ldots \\
0 & \ddots & 0 \\
0 & \ldots & \frac{1}{L_N}
\end{bmatrix}
\]
\[ (3.5) \]
with the abbreviations \( Y_o := \frac{R_l}{R_C + R_l} \), and \( Z_t := Y_o R C \sum_{n=1}^{N} \frac{1}{L_n} \) are readily obtained.

### 3.2 Sliding Surface Definition

Following the modeling process of the \( N \)-phase converter as a VSS in Section 3.1, a digital control structure for the SMPS is presented in this section. The control structure can be divided into two parts, whereby both of them are discussed in the following paragraphs. Firstly, an SMC approach achieving the main objectives of output voltage regulation and current balancing between the phases is proposed. Secondly, a dynamic hysteresis modulation scheme for fixed-frequency and interleaved operation is presented.

As anticipated, one of the control objectives is to regulate the output voltage to the desired reference value \( V_{\text{ref}} \). To achieve this, the control law has to force the output voltage error \( v_e(t) := (v_{\text{out}}(t) - V_{\text{ref}}) \) towards zero by appropriately toggling the control signals \( c_n(t) \). With SMC, this can be achieved by defining a vector \( \sigma(x_e(t)) \in \mathbb{R}^{N \times 1} \) of sliding functions \( \sigma_n(x_e(t)) \) and expressing the control goal as
\[
\sigma(x_e(t)) = Gx_e(t) = 0.
\]
\[ (3.6) \]
In (3.6), \( G \) and \( x_e(t) \) denote the, yet to be defined, gain matrix and state vector, respectively. With this definition, the sliding functions are time-invariant and linear combinations of the states, which facilitates a low-complexity implementation. Furthermore, it is worth noting that the state vector \( x_e(t) \) does not necessarily correspond to
the natural states of the converter. Rather, it is chosen in such a way that the desired control goal is expressed. For the \(N\)-phase converter depicted in Figure 3.1, the state vector

\[
x_c = \begin{bmatrix}
v_e(t) \\
i_{L_1}(t) \\
\vdots \\
i_{L_N}(t) \\
\int v_e(t) \, dt \\
\int (i_{L_1}(t) - \bar{i}_L(t)) \, dt \\
\vdots \\
\int (i_{L_N}(t) - \bar{i}_L(t)) \, dt
\end{bmatrix} \in \mathbb{R}^{(2N+2) \times 1}
\]

(3.7)
is proposed. In order to achieve regulation towards the desired output voltage \(V_{\text{ref}}\), the state \(v_e(t)\) is used. To improve the dynamic performance, the inductor currents \(i_{L_n}(t)\) are incorporated in the state vector. Using the inductor currents instead of the capacitor current \(i_C(t)\) allows for a unified definition of the sliding surface, since \(i_C(t)\) is not continuous for all converter types [25], [26]. Furthermore, the integrator state \(\int v_e(t) \, dt\) ensures that any steady state error in the output voltage, e.g., caused by the typically nonzero average inductor currents or by a finite switching frequency, is removed.

Parameter variations of the individual phases, such as different values of the parasitic resistances \(R_{p_n}\), might result in unequal sharing of the load current \(i_l(t)\) among the phases. Hence, thermal stress is unequally distributed between the phases, possibly degrading reliability [90]. Therefore, equal current sharing is often desired in multiphase converters. With the proposed SMC this is accomplished by introducing the states \(\int (i_{L_n}(t) - \bar{i}_L(t)) \, dt\), with \(\bar{i}_L(t) := \frac{1}{N} \sum_{n=1}^{N} i_{L_n}(t)\).

From (3.7), it is evident that the control law requires current information. While for the states \(i_{L_n}(t)\) the high-frequency AC current ripples are relevant, the DC components of the inductor currents are sufficient for current balancing [90]. By reconstructing the AC waveforms digitally, the implementation effort can be significantly reduced, since then no current ADCs with high sampling rates are required [61]. The design of an SMO for the proposed control scheme is outlined in Chapter 4. Furthermore, by additionally estimating \(R_{p_n}\), current sensing can be completely avoided [90]–[93].

After the state vector has been defined, appropriate switching decisions must be selected. For the state vector (3.7), the switching decisions

\[
c_n(t) = \begin{cases} 
    c^-_n(t) & : 0 & \text{ if } \sigma_n(x_c(t)) > 0 \\
    c^+_n(t) & : 1 & \text{ if } \sigma_n(x_c(t)) < 0 
\end{cases}
\]

(3.8)
which direct the state vector $x_c(t)$ towards the sliding surface, immediately follow. Here, $c_n(t)$ and $\sigma_n(x_c(t))$ denote the control signal and the sliding surface of the $n$th phase, respectively.

Due to the change of the state vector from $x(t)$ to $x_c(t)$, the system model (3.1) has to be rewritten as

$$\dot{x}_c(t) = A_c x_c(t) + B_c c(t) + D_c,$$  \hspace{1cm} (3.9)

with the augmented system matrix $A_c \in \mathbb{R}^{(2N+2)\times(2N+2)}$, the new input matrix $B_c \in \mathbb{R}^{(2N+2)\times N}$, and the vector $D_c \in \mathbb{R}^{(2N+2)\times 1}$, which accounts for the coordinate system transformation from $v_{out}(t)$ to $v_c(t)$. In (3.9),

$$A_c = \begin{bmatrix} 1 & 0 & \cdots & \cdots & 0 \\ 0 & (1 - \frac{1}{N}) & -\frac{1}{N} & \cdots & -\frac{1}{N} \\ \vdots & -\frac{1}{N} & \ddots & \ddots & \vdots \\ \vdots & \vdots & \ddots & \ddots & -\frac{1}{N} \\ 0 & -\frac{1}{N} & \cdots & -\frac{1}{N} & (1 - \frac{1}{N}) \end{bmatrix},$$  \hspace{1cm} (3.10)

$$B_c = \begin{bmatrix} B \\ 0 \end{bmatrix},$$  \hspace{1cm} (3.11)

and

$$D_c = \begin{bmatrix} -V_{ref} \left( R_t + \frac{R_o}{C_R} \right) \\ -\frac{V_{ref}}{L_t} \\ \vdots \\ -\frac{V_{ref}}{L_N} \\ 0 \end{bmatrix}.$$  \hspace{1cm} (3.12)

The sliding surface vector (3.6) is a linear combination of the states $x_c(t)$, where the gain matrix $G \in \mathbb{R}^{N\times(2N+2)}$ decides their weighting. For the system description (3.9),

$$G = \begin{bmatrix} g_1 \\ \vdots \\ g_2 I_N, \quad \vdots \\ g_3 I_N \end{bmatrix}.$$  \hspace{1cm} (3.13)

is proposed. Thus, the inductor current $i_{L_n}(t)$ and the current balancing term $\int (i_{L_n}(t) - \bar{i}_L(t)) \, dt$ only appear in the sliding function $\sigma_n(x_c(t))$ of the $n$th phase. As will be shown later, such a definition of $G$ has two convenient properties. Firstly, the proportional and integral parts are common to all phases. Thus, it is not necessary to
individually compute them for every phase. Secondly, the controller
design can be carried out separately for the voltage control loop and
a current balancing control, which simplifies the process.

The proposed definition of the gain matrix $G$ allows for a straight-
forward design of the controller coefficients. Utilizing the equivalent
control method [18], [24], an equivalent continuous control command
c_{eq}(t)$ for the discontinuous input vector $c(t)$ in (3.9) is derived. Con-
secutively, the closed-loop dynamics are calculated. Under sliding
regime $\sigma(x_c(t)) = 0$ and $\dot{\sigma}(x_c(t)) = 0$ hold and hence

$$\dot{x}_c(t) = \frac{\partial (Gx_c(t))}{\partial x_c(t)} x_c(t) = G \dot{x}_c(t) = 0. \quad (3.14)$$

Substituting $\dot{x}_c(t)$ in (3.14) with the RHS of (3.9) and solving for $c(t)$,
yields the equivalent control

$$c_{eq}(t) = - (GB_c)^{-1} (GA_c x_c(t) + GD_c). \quad (3.15)$$

Consequently, by replacing $c(t)$ in (3.9) with the RHS of (3.15), the
closed-loop dynamics of the converter under SMC are given by

$$\dot{x}_c(t) = A_c x_c(t) + B_c c_{eq}(t) + D_c$$
$$= A_c x_c(t)$$
$$- B_c \left( (GB_c)^{-1} (GA_c x_c(t) + GD_c) + D_c \right)$$
$$= \left( A_c - B_c (GB_c)^{-1} GA_c \right) x_c(t)$$
$$- B_c (GB_c)^{-1} GD_c + D_c. \quad (3.16)$$

Thus, the controller coefficients can be obtained by calculating the
characteristic polynomial $p_{A_{eq}}(s)$ of the closed-loop system matrix
$A_{eq}$. Due to the order reduction property of SMC and the choice of $G$
as in (3.13), the closed-loop system is of order $(N + 1)$ and the charac-
teristic polynomial can be factorized in $p_{A_{eq}}(s) = p_{A_{eq,vc}}(s) p_{A_{eq,cb}}(s)$,
yielding

$$p_{A_{eq,vc}}(s) = s^2 + \alpha (g_1NR_i + g_2 + g_3NCR_CR_i) s$$
$$+ g_3NR_i \alpha, \quad (3.17)$$

with $\alpha := \frac{1}{c(g_2R_C + g_3R_i + g_1R_CC_R)}$, and

$$p_{A_{eq,cb}}(s) = \left( g_4 + g_2s \right)^{(N-1)} \frac{g_2(N-1)}{g_2}. \quad (3.18)$$

By letting $g_2 = 1$, $p_{A_{eq,vc}}(s)$ and $p_{A_{eq,cb}}(s)$ can be used to design
the output voltage regulation and current balancing loop, respectively.
Equating (3.17) and (3.18) with the desired polynomials and solving
for $g_1$, $g_3$, and $g_4$, yields the required controller gains.
In addition to guaranteeing stability, the gain matrix $G$ must be chosen in such a way that the reaching and existence conditions are met. While the former ensures that the sliding surface is reached, the latter defines the region in state space for which a sliding mode exists. The reaching and existence conditions for the $n$th sliding surface can be expressed as

$$
\dot{\sigma}_n (x_c (t)) = \begin{cases} 
g_n \dot{x}_c (t) \leq -\eta & \text{if } \sigma_n (x_c (t)) > 0 
g_n \dot{x}_c (t) \geq \eta & \text{if } \sigma_n (x_c (t)) < 0 
\end{cases},
$$

with $g_n$ denoting the $n$th row of $G$,

$$
x_c^\pm (t) := Ax_c (t) + b_n c_n^\pm (t) + D,
$$

and the strictly positive constant $\eta$, which ensures finite time reachability of the sliding surface. In (3.20), $b_n$ refers to the $n$th column of $B$. For the reaching conditions, (3.19) is evaluated with the phase currents neglected, since $v_c (t)$ dominates $\dot{\sigma}_n (x_c (t))$ if the state vector is far from the sliding surface. In contrast to the derivation for the reaching conditions, $v_c (t)$ almost vanishes near the sliding surface, hence it can be neglected for the existence conditions.

While the derivation of the closed-loop dynamics $A_{eq}$ has been carried out in CT, the actual controller is implemented as a DT system with a clock rate $\frac{1}{T_{digi}} \gg \frac{1}{T_{sw}}$. Hence, by applying forward Euler discretization to (3.6), with $x_c (t)$ and $G$ as defined in (3.7) and (3.13), respectively, the DT vector of sliding functions

$$
\sigma_m (x_{c,m}) = G_d (x_{c,m} + x_{i,m})
$$

is readily obtained. In (3.21), the subscript $m$ denotes the $m$th sample obtained with the digital clock rate $\frac{1}{T_{digi}}$, and $x_{i,m}$ refers to the $i$th row of $x_{c,m}$. For high sampling rates in comparison with the switching
frequency and natural dynamics of the plant, this method provides a simple, yet accurate, method of discretization [95]. Further note that, the chosen discretization is not equivalent to an SMC law for a DT plant, e.g., obtained by a ZOH discretization of a CT system.

The switching decisions in DT are given by

\[
c_{n,m} = \begin{cases} 
  c_{n,m}^- := 0 & \text{if } \sigma_{n,m}(x_{c,m}) > h_{n,m} \\
  c_{n,m}^+ := 1 & \text{if } \sigma_{n,m}(x_{c,m}) < -h_{n,m} \\
  c_{n,(m-1)} & \text{else}
\end{cases}
\]  \tag{3.22}

Note that, as already anticipated by Figure 3.1, the switching decisions given by (3.22) include a hysteresis window of width \(2h_{n,m}\).

The objective of this hysteresis window is to obtain a finite switching frequency, which is necessary for a practical implementation. In Section 3.3, the influence of the hysteresis width on the switching frequency and phase shift is outlined in detail, and a dynamic hysteresis modulation scheme is proposed.

The structure of the proposed digital controller is reported in Figure 3.3. The output voltage error and its cumulative sum is common to all phases, hence, they are calculated only once for each sampling point \(m\). In Figure 3.3, the sum of these two components is denoted as \(\sigma_{c,m}(x_{c,m})\). To obtain the sliding surface \(\sigma_{n,m}(x_{c,m})\) of each phase \(n\), the inductor current \(i_{L,n,m}\) scaled by \(g_{d2}\) and a current balancing offset are added to \(\sigma_{c,m}(x_{c,m})\), as shown in Figure 3.3b. Finally, the control signal \(c_{n,m}\) is generated based on (3.22).
3.3 Dynamic Hysteresis Modulation

By defining a constant value for $h_{n,m}$, the switching frequency can be limited. Nevertheless, varying operating conditions, such as different input voltage and load current levels, cause a non-constant switching frequency. Furthermore, interleaving cannot be achieved, since there is no control over the phase shift of the switching signals. In order to obtain a constant switching frequency and interleaving independent of the operating conditions, it is necessary to dynamically adapt $h_{n,m}$.

In the following, a novel hysteresis control scheme, achieving both requirements, is presented.

3.3.1 Fixed-frequency operation

In [42], [59], control schemes for achieving fixed-frequency operation have been proposed. Therein, a control loop is used to adapt the hysteresis width depending on the switching period error $T_{sw,k} := (T_{sw,ref} - T_{sw,n,k})$ between the measured duty cycle $T_{sw,n,k}$ in the $k$th switching period and the desired reference $T_{sw,ref}$. This work follows a similar approach, whereas the control loop is employed to every phase of the multi-phase converter. Additionally, a small-signal model for the hysteresis width to switching period $T_F H_{T_{sw}}(z) = T_{sw,n}^{+} + h_{n,m}^{+}$ for the chosen sliding surface definition, introduced in Section 3.2, is derived.

In Figure 3.4a, the influence of the hysteresis value $h_{n,k}$ on the switching frequency $T_{sw,n,k}$ is illustrated. The subscript $k$ denotes the $k$th switching period. Hence, the hysteresis value is only updated once per switching period in the illustrated scheme. During the on-time $T_{on}$ ($c_{n,m} = c_{n,m}^{+}$), the sliding surface $\sigma_{n,m}(x_{c,m})$ increases with the slope

$$\dot{\sigma}_{n,k}^{+} := \frac{\sigma_{n}^{+}(x_{c,m}) - \sigma_{n}^{+}(x_{c,(m-1)})}{T_{digi}},$$

whereas during the off-time $T_{off}$ ($c_{n,m} = c_{n,m}^{-}$), the slope is given by

$$\dot{\sigma}_{n,k}^{-} := \frac{\sigma_{n}^{-}(x_{c,m}) - \sigma_{n}^{-}(x_{c,(m-1)})}{T_{digi}}.$$  \hspace{1cm} (3.24)

Since the switching decision between the on- and off-state is governed by (3.22), the period of the $k$th switching cycle is given by

$$T_{sw,n,k} = \frac{h_{n,k} + h_{n,(k-1)}}{\dot{\sigma}_{n,k}^{+}} - \frac{2h_{n,k}}{\dot{\sigma}_{n,k}^{-}}.$$  \hspace{1cm} (3.25)

In (3.25), an update of the hysteresis width occurs once per switching period, with the rising edge of $c_{n,m}$. Also, $\dot{\sigma}_{n,k}^{+}$ and $\dot{\sigma}_{n,k}^{-}$ are assumed to
Figure 3.4: Influence of the hysteresis width on the switching period length and the delay.

be constant during $T_{on}$ and $T_{off}$, respectively. Moreover, recalling that $\sigma_m(x_{c,m}) = G_d(x_{c,m} + x_{i,m})$, the slopes $\dot{\sigma}_{n,k}^{\pm}$ are given by

$$
\dot{\sigma}_{n,k}^{\pm} = \frac{g_{d,n}}{T_{sw,n,k}} \left( x_{c,m} - x_{c,(m-1)} + x_{i,m} - x_{i,(m-1)} \right) 
= \frac{g_{d1}}{T_{sw,n,k}} \left( v_{c,m} - v_{c,(m-1)} \right) 
+ \frac{g_{d2}}{T_{sw,n,k}} \left( i_{L_a,m} - i_{L_a,(m-1)} \right) 
+ \frac{g_{d3}}{T_{sw,n,k}} \left( v_{c,(m-1)} - v_{c,(m-2)} \right) 
+ \frac{g_{d4}}{T_{sw,n,k}} \left( i_{L_a,(m-1)} - i_{L_a,(m-2)} \right) 
+ \frac{g_{d4}}{T_{sw,n,k}} \left( \hat{i}_{L,(m-1)} - \hat{i}_{L,(m-2)} \right) 
+ \frac{g_{d4}}{T_{sw,n,k}} \left( x_{i,m} - x_{i,(m-1)} \right),
$$

Since the controller regulates the output voltage to the desired reference, and balances the phase currents, $v_{out,m} \approx V_{ref}$ and $i_{L_a,m} \approx \hat{i}_{L,m}$ is assumed during steady state. Therefore, the steady state slopes of the
sliding functions can be approximated by the inductor current slopes

\[
\dot{\sigma}_{ss,n}^+ \approx \frac{g_{d2}}{T_{sw,n,k}} \left( i_{L,n,m} - i_{L,n,(m-1)} \right) \\
\approx \left( \frac{i_{L,n,(m-1)}}{T_{sw,n,k}} - \frac{V_{in,(m-1)} - V_{out,(m-1)}}{L_n} - \frac{i_{L,n,(m-1)}}{T_{sw,n,k}} \right) \\
\approx \frac{V_{in} - V_{out}}{L_n},
\]

\[
\dot{\sigma}_{ss,n}^- \approx \frac{g_{d2}}{T_{sw,n,k}} \left( i_{L,n,m} - i_{L,n,(m-1)} \right) \\
\approx \left( \frac{i_{L,n,(m-1)}}{T_{sw,n,k}} - \frac{V_{out,(m-1)}}{L_n} - \frac{i_{L,n,(m-1)}}{T_{sw,n,k}} \right) \\
\approx \frac{V_{out}}{L_n},
\]

whereby, without loss of generality, \( g_{d2} = 1 \) has been assumed. Consequently, since \( \dot{\sigma}_{ss,n}^\pm \) are no longer time-varying, the DT TF

\[
H_{T_{sw,n}}(z) = \frac{T_{sw,n}(z)}{h_n(z)} = \frac{1 + z^{-1}}{\dot{\sigma}_{ss,n}^+ - \dot{\sigma}_{ss,n}^-}
\]

is obtained by substituting \( \dot{\sigma}_{n}^\pm \) in (3.25) with the approximations \( \dot{\sigma}_{ss,n}^\pm \) derived in (3.27) and performing a z-transformation. In (3.28), the sampling time equals the length of one nominal switching period \( T_{sw} \). Further note that, from (3.25), the constant hysteresis value

\[
h = \frac{T_{sw}\dot{\sigma}_{ss}^+\dot{\sigma}_{ss}^-}{2(\dot{\sigma}_{ss}^+ - \dot{\sigma}_{ss}^-)}
\]

which yields a steady state switching period length of \( T_{sw} \) for the nominal system parameters, can be readily derived.

### 3.3.2 Interleaving operation

To achieve interleaving in a multi-phase converter, in addition to the constant switching frequency requirement, the control signals \( c_{n,m} \) have to be delayed by \( T_{sw} \) with respect to each other. Conventional hysteresis SMC implementations constrain the number of phases for a certain operating condition by (2.118). In the following, a novel method for accomplishing the phase shift regardless of the number of phases and operating conditions is presented. To that end, an additional hysteresis width control loop is employed. The objective of this phase regulation loop is to modulate the hysteresis width of the \( (n+1) \text{th} \) phase in such a way that the delay error \( \Phi_{n,(n+1),k} := \left( \Phi_{ref} - \Phi_{n,(n+1),k} \right) \) between the phases \( n \) and \( (n+1) \) vanishes. Here,
\( \Phi_{\text{ref}} := \frac{T_{sw}}{h} \) denotes the required phase shift to achieve interleaving and \( \Phi_{n,(n+1),k} \) is the measured delay in the \( k \)th switching period.

In Figure 3.4b, the impact of the hysteresis width \( h_{(n+1),k} \) on the delay \( \Phi_{n,(n+1),k} \) between two phases \( n \) and \( (n + 1) \) is depicted. For illustration purposes, \( h_{n,k} \) is held constant. At the beginning of the \((k-1)\)th switching cycle, \( n \) and \( (n + 1) \) are in-phase. For \( h_{n,k} = h_{(n+1),k} \) and \( \dot{\sigma}_{ss,n} = \dot{\sigma}_{ss,(n+1)} \), it follows that \( T_{sw,n,(k-1)} = T_{sw,(n+1),(k-1)} \). Hence, the two phases are also in-phase at the beginning of the \( k \)th switching cycle. As a consequence of increasing \( h_{(n+1),k} \) in the \( k \)th switching cycle, \( T_{sw,(n+1),k} \) also increases. Moreover, due to the increased period length of the phase \((n + 1)\), the turn-on time of \( c_{(n+1),m} \) is delayed by \( \Phi_{n,(n+1),(k+1)} \) with respect to \( c_{n,m} \) in the \((k + 1)\)th switching cycle. Therefore, the delay \( \Phi_{n,(n+1),k} := \left( T_{sw,(n+1),k} - T_{sw,n,k} \right) \) can be expressed as

\[
\Phi_{n,(n+1),k} = \Phi_{n,(n+1),(k-1)} + \Delta h_{n,(n+1),(k-1)} + \Delta h_{n,(n+1),k} - \frac{2\Delta h_{n,(n+1),k}}{\dot{\sigma}_{ss}}, \tag{3.30}
\]

with \( \Delta h_{n,(n+1),k} := (h_{(n+1),k} - h_{n,k}) \) and the constant slopes \( \dot{\sigma}_{ss} = \dot{\sigma}_{ss,n} = \dot{\sigma}_{ss,(n+1)} \) during \( T_{on} \) and \( T_{off} \). Consequently, by \( z \)-transforming (3.30), the hysteresis width delta \( \Delta h_{n,(n+1),k} \) to delay \( \Phi_{n,(n+1),k} \) TF

\[
H_{\Phi_{n,(n+1)}}(z) = \frac{\Phi_{n,(n+1)}(z)}{\Delta h_{n,(n+1)}(z)} = \frac{1 + z^{-1}}{\dot{\sigma}_{ss} (1 - z^{-1})} - \frac{2}{\dot{\sigma}_{ss} (1 - z^{-1})} \tag{3.31}
\]

with sampling time \( T_{sw} \) is readily obtained.

### 3.3.3 Control approach

With the derived TFs (3.28) and (3.31) it is possible to design two control loops for maintaining a constant switching frequency and phase shift. A digital dual loop control concept is reported in Figure 3.5. The controllers \( C_{T_{sw}}(z) \) and \( C_{\Phi}(z) \) are used to achieve a constant frequency and interleaving, respectively. The switching period \( T_{sw,n,k} \) of the \( n \)th phase is measured by a counter, reset at each rising edge of \( c_{n,m} \). In a similar way, the delay \( \Phi_{n,(n+1),k} \) is obtained, whereas the counter is reset with the rising edge of \( c_{n,m} \) and stopped with the rising edge of \( c_{(n+1),m} \). Note the delay in the feedback path of the frequency control loop. This delay is inherently included due to the way the switching period is measured. In other words, the measurement of the switching period of the \( k \)th period is available after the period
has ended, which is the beginning of the \((k+1)\)th switching cycle, hence the delay.

3.4 Simulation Results

In order to verify the proposed control approach, simulations for the two-phase buck converter introduced in Section 2.2.3 have been carried out. For convenience, the nominal parameters are reported in Table 3.1 once again. A two-phase buck converter has been selected since constraint (2.118) is never fulfilled for such a topology. Thus, as already elaborated, other hysteresis SMC approaches fail to achieve the required delay of \(T\) for interleaving.

Utilizing (3.17) and (3.18), the controller gains have been calculated to yield a closed-loop bandwidth of \(\omega_{SMC} = 2\pi \cdot 55\) kHz and a damping factor of \(\zeta_{SMC} = 0.7\). Furthermore, an integral (I) compensator has been used for the frequency controller \(C_T\) (z), while \(C_{\Phi} (z)\) employs a PI controller to obtain the required phase shift. The controllers \(C_T\) and \(C_{\Phi}\) have been tuned to obtain a closed-loop bandwidth of \(\omega_T = 2\pi \cdot 25\) kHz and \(\omega_{\Phi} = 2\pi \cdot 30\) kHz, respectively, with

### Table 3.1: Two-phase buck converter parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{in})</td>
<td>3.3 V</td>
<td>(L_1, L_2)</td>
<td>3.3 (\mu)H</td>
</tr>
<tr>
<td>(C)</td>
<td>20 (\mu)F</td>
<td>(R_{p_1}, R_{p_2})</td>
<td>220 m(\Omega)</td>
</tr>
<tr>
<td>(R_C)</td>
<td>10 m(\Omega)</td>
<td>(I_l)</td>
<td>0 A - 2 A</td>
</tr>
<tr>
<td>(V_{ref})</td>
<td>1.25 V</td>
<td>(f_{sw})</td>
<td>1.5625 MHz</td>
</tr>
<tr>
<td>(f_d)</td>
<td>100 MHz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
damping factors of $\zeta_{T_{\text{sw}}} = \zeta_{\Phi} = 1$. Hence, the SMC reacts faster to changes in the operating conditions than the frequency and phase shift controllers, and a variable frequency and phase shift can occur during transient events. In Table 3.2, the design parameters of the proposed SMC approach are summarized.

Firstly, the frequency responses of the analytical TFs (3.28) and (3.31) have been validated by comparing them to the responses obtained from a MATLAB simulation. To that end, a static hysteresis width has been perturbed by a sinusoidal stimulus at different frequencies. Then, the Fourier coefficients of $h_{n,k}$, $T_{\text{sw},n,k}$ and $\Phi_{n,(n+1),k}$ have been evaluated at these frequencies in order to obtain the simulated frequency responses [47]. In Figure 3.6a, the magnitude and phase response of $H_{T_{\text{sw}},n} \frac{z-1}{\text{dig}} (z)$ are reported. As already discussed, the delay stems from the fact that the length of the switching period is only known at its end. As predicted by the analytical model, this delay manifests itself as a phase lag at higher frequencies, which is confirmed by the MATLAB simulation. The magnitude and phase response of $H_{\Phi_{n,(n+1),k}} \frac{1}{\text{dig}} (z)$ are shown in Figure 3.6b. The integrative behavior, as described in Section 3.3.2, can be observed. The MATLAB simulation confirms the analytical model of both TFs. Hence, (3.28) and (3.31) serve as a starting point for designing the frequency and phase loop, respectively.

Secondly, the performance of the frequency and phase loop has been evaluated by applying line and load variations. The output voltage, switching period, and delay responses to a line drop from 5 V to the nominal value of 3.3 V, occurring at $t = 1 \mu s$, are reported in Figure 3.7. While the output voltage stays almost constant for all three configurations, the reduced ripple magnitude, caused by interleaving, is clearly visible for the configuration with activated phase loop ($C_{T_{\text{sw}}}(z) & C_{\Phi}(z)$). As can be seen in Figure 3.7b, a reduced input voltage results in an increased switching period, hence the switching frequency decreases. Clearly, both the frequency loop alone and the frequency loop with the additional phase loop are able to restore the desired switching frequency after a transient time. Moreover, as Figure 3.7c illustrates, the proposed phase control loop maintains the desired delay between the two phases. Note that, without the phase control loop activated, the delay is constantly zero. Therefore, Fig-

<table>
<thead>
<tr>
<th>Controller</th>
<th>Bandwidth</th>
<th>Value</th>
<th>Damping Factor</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sliding Mode</td>
<td>$\omega_{\text{SMC}}$</td>
<td>$2\pi \cdot 55 \text{kHz}$</td>
<td>$\zeta_{\text{SMC}}$</td>
<td>0.7</td>
</tr>
<tr>
<td>$C_{T_{\text{sw}}}(z)$</td>
<td>$\omega_{T_{\text{sw}}}$</td>
<td>$2\pi \cdot 25 \text{kHz}$</td>
<td>$\zeta_{T_{\text{sw}}}$</td>
<td>1.0</td>
</tr>
<tr>
<td>$C_{\Phi}(z)$</td>
<td>$\omega_{\Phi}$</td>
<td>$2\pi \cdot 30 \text{kHz}$</td>
<td>$\zeta_{\Phi}$</td>
<td>1.0</td>
</tr>
</tbody>
</table>
3.4 Simulation Results

(a) Validation of the hysteresis width to switching period frequency response of the TF $H_{\text{sw},n}(z) z^{-1}_{\text{dig}}$.

(b) Validation of the hysteresis width to delay frequency response of the TF $H_{\Phi,n+1} \frac{1}{T_{\text{dig}}}(z)$.

Figure 3.6: Comparison of the analytically derived hysteresis width TFs with simulation results.
Figure 3.7c omits the configurations with a static hysteresis ($h_{\text{const}}$) and only the frequency control loop employed ($C_{T_{\text{sw}}}(z)$).

In Figure 3.8, the output voltage, switching period, and delay during a load jump from 0 A to 2 A, occurring at $t = 1 \mu s$, can be seen. As reported in Figure 3.8a, the additional control loops have virtually no impact on the transient response of $v_{\text{out}}(t)$. As for the line drop, both constant switching frequency and phase shift are restored after a short transient by the frequency and phase loop, respectively. Moreover, without the additional phase control loop, the phases are not interleaved, i.e., $\Phi_{1,2,k} = 0$, and hence, Figure 3.8c reports the delay transient with activated phase control loop only.

Finally, the step response of $\Phi_{1,2,k}$ to a step change of the reference $\Phi_{\text{ref}}$ from 0 s to the desired value of $T_{\text{sw},2}$, occurring at $t = 1 \mu s$, has been evaluated. As can be seen in Figure 3.9b, the hysteresis $h_{2,k}$ of the second phase is increased by the phase control loop. Hence, the switching period $T_{\text{sw},2,k}$ also increases, as reported in Figure 3.9c. As desired, the dynamic hysteresis modulation results in a delay between the first and the second phase, as shown in Figure 3.9d and Figure 3.9e. The delay causes interleaved operation, which in turn reduces the output voltage ripple, as illustrated in Figure 3.9a.
Figure 3.7: Behavior of the different hysteresis modulation schemes during a line drop from 5 V to 3.3 V.
Figure 3.8: Behavior of the different hysteresis modulation schemes during a load jump from 0 A to 2 A.
3.4 SIMULATION RESULTS

(a) Response of the output voltage.

(b) Response of the sliding function.

(c) Response of the switching period.
Figure 3.9: Behavior of the proposed hysteresis modulation scheme during a step change of $\Phi_{\text{ref}}$ from 0 s to $\frac{T_{\text{sw}}}{2}$.
CURRENT RECONSTRUCTION SLIDING MODE OBSERVER

As illustrated in Figure 3.3b, the sliding surface calculation requires the inductor currents of each phase [24]. In case of a digital controller implementation, in addition to the current sensor, an ADC with a high sampling rate is required, which increases the implementation effort significantly. Hence, because of the reduction of required hardware, digitally estimating the current would provide an attractive alternative. Many inductor current estimation approaches, such as the ones introduced in [90]–[93], estimate the DC components of the phase currents only, which is sufficient for current balancing. However, the AC switching ripple components of $i_{L_n} \forall n \in \{1, \ldots, N\}$ are necessary for the sliding mode controller. A common challenge in AC current reconstruction schemes is the drift of the estimated inductor current. Due to quantization, sampling, and mismatches between the component values of the real converter and the estimator, the volt-second balance is typically violated for the current reconstruction algorithm. Without compensation, this in turn causes the estimated current to grow without bounds instead of following the real inductor current waveform [62]. In [96], a digital current reconstruction for a $V^2$ controlled single-phase buck converter has been presented. In order to prevent drifting of the estimated current caused by modeling mismatches, quantization, and sampling effects, a compensator is proposed therein. Another drift compensation method for a single-phase buck converter with a sliding mode controller has been used in [26], but no insight on the compensator design and influence of parameter variations is given.

In this work, a novel digital SMO that obtains the required AC current information is proposed. No additional drift compensation is necessary, and the estimated current can be directly used by the sliding mode controller. The efficient digital implementation of the observer only requires sensing of the output voltage. Furthermore, it is possible to additionally sense the input voltage, which improves the robustness against line jumps. Again, simulation results for a two-phase buck converter are provided in order to demonstrate the effectiveness of the presented approach.
4.1 OBSERVER DESIGN

In accordance with the VSS model of the converter derived in Section 3.1, the CT equation of the SMO can be written as

\[ \dot{x}(t) = A\hat{x}(t) + Bc(t) + k \, \text{sgn}(v_{\text{out}}(t) - \hat{v}_{\text{out}}(t)), \]  

with the state vector estimate \( \hat{x}(t) \in \mathbb{R}^{(N+1) \times 1} \), estimated output voltage \( \hat{v}_{\text{out}}(t) \) and observer gain vector

\[ k = [k_1, k_2, \ldots, k_{(N+1)}]^T \in \mathbb{R}^{(N+1) \times 1}. \]

Since only the natural states of the converter have to be estimated, \( \hat{x}(t) \) is defined analogous to (3.2). Furthermore, \( A \) and \( B \) are given by (3.4) and (3.5), respectively. With the error between the true state vector and its estimate defined as \( e(t) := (x(t) - \hat{x}(t)) \), it is easily verified that the dynamics of the estimation error yield

\[ \frac{de(t)}{dt} = \frac{d(x(t) - \hat{x}(t))}{dt} = Ax(t) + Bc(e) - (A\hat{x}(t) + Bc(e) + k \, \text{sgn}(v_{\text{out}}(t) - \hat{v}_{\text{out}}(t))) = Ae(t) - k \, \text{sgn}(e_1(t)), \]

with \( e_1(t) \) denoting the first element of \( e(t) \). Note that, the state vector \( x(t) \), as well as its estimate \( \hat{x}(t) \), only contains the natural state variables of the converter, whereas the augmented state vector \( x_c(t) \) introduced in Section 3.2 is used by the sliding mode controller only. The objective of the SMO is now to direct the output voltage estimation error \( e_1(t) \) towards the origin. Similar to SMC, as reviewed in Section 2.3, this can be expressed as

\[ \sigma_0(e_1(t)) = e_1(t) = 0, \]

with the sliding function \( \sigma_0(e_1(t)) \) of the SMO. The existence of the sliding mode can then be shown by choosing the Lyapunov function candidate

\[ V(e_1(t)) = \frac{1}{2}e_1^2(t). \]

\( V(e_1(t)) \) and its time-derivative

\[ \dot{V}(e_1(t)) = \frac{\partial V(e_1(t))}{\partial e_1(t)} \dot{e}_1(t) = e_1(t) \dot{e}_1(t) \]

have to be positive and negative definite, respectively, in order to fulfill the existence condition [24], [26]. Since

\[ \dot{V}(e_1(t)) = e_1(t) \dot{e}_1(t) = e_1 \left( a_1^T e(t) - k_1 \, \text{sgn}(e_1(t)) \right), \]
with $a_1^T$ being the first row vector of $A$, the conditions

$$k_1 > \begin{cases} + a_1^T e(t) & \text{if } e_1(t) > 0 \\ - a_1^T e(t) & \text{if } e_1(t) < 0, \end{cases}$$ (4.8)

which are required for $V(e_1(t)) < 0$ to hold, can be derived. Note that, positive definiteness of $V(e_1(t))$ is guaranteed for $e_1(t) \neq 0$ due to its definition given by (4.5). Hence, (4.8) is obtained by setting the RHS of (4.7) equal to 0 and solving for $k_1$, whereby the two cases $e_1(t) > 0$ and $e_1(t) < 0$ have to be considered separately. It immediately follows from (4.8) that the gain $k_1$ has to be chosen such that

$$k_1 > \max |a_1^T e|$$ (4.9)

holds. Here, $\max |a_1^T e|$ denotes the maximum estimation error of the output voltage, which can be obtained from the converter parameters and simulations.

For calculating the closed-loop error dynamics under sliding regime and consequently the gains $k_{2,\ldots,(N+1)}$, the equivalent control method reviewed in Section 2.3.3 is utilized. By substituting $\text{sgn} (e_1(t))$ in (4.3) with $u_{\text{eq}}(t)$, the error dynamics under equivalent control can be written as

$$\frac{de(t)}{dt} = Ae(t) - ku_{\text{eq}}(t).$$ (4.10)

During sliding mode operation, $\sigma_o(e_1(t)) = \dot{\sigma}_o(e_1(t)) = 0$ holds. Furthermore, as immediately follows from (4.4), $e_1(t) = \dot{e}_1(t) = 0$, and thus

$$u_{\text{eq}} = \frac{1}{k_1} a_1^T e(t) = \frac{1}{k_1} \begin{bmatrix} a_2 & \ldots & a_{(N+1)} \end{bmatrix} \begin{bmatrix} e_2(t) \\ \vdots \\ e_{(N+1)}(t) \end{bmatrix}$$ (4.11)

is obtained from the first row of (4.3). In (4.11), $a_i$ denotes the $i^{th}$ element of $a_1^T$. Substituting the RHS of (4.11) for $u_{\text{eq}}(t)$ into the $N$ remaining non-zero rows of (4.10), yields the reduced order error dynamics

$$\dot{e}_r(t) = A_r e_r(t) - \begin{bmatrix} k_2 \\ \vdots \\ k_{(N+1)} \end{bmatrix} u_{\text{eq}}(t)$$ (4.12)

$$= A_r e_r(t) - k_r a_r^T e_r(t) = \left( A_r - k_r a_r^T \right) e_r(t),$$
whereby $A_r$ is composed of $A$ with the first row and column removed. The observer dynamics are now defined by $A_{r,\text{eq}}$. In order to stabilize the error dynamics (4.12) and thus the SMO (4.1), the eigenvalues of the matrix $A_{r,\text{eq}}$ are required to have a negative real part, which can be achieved by appropriate choice of the gain vector $k_r$. By computing the unique solution $P$ of the CT algebraic Riccati equation [51]

$$A_rP + PA_r^T - P a_r R^{-1} a_r^T P + Q = 0,$$

with the resulting feedback gain defining positive definite cost parameters $Q, R$, and choosing

$$k_r = R^{-1} P a_r,$$

a stable SMO is obtained.

For the digital implementation of the SMO, (4.1) is converted to DT, yielding the system of difference equations

$$\dot{\hat{x}}_{m+1} = \Phi \hat{x}_m + \Gamma c_m + k_{d} \text{sgn}(e_{1,m}),$$

which is used to update the estimated state vector $\hat{x}_m$ with the high digital clock rate $\frac{1}{T_{\text{digi}}}$. In (4.15),

$$\Phi = e^{A T_{\text{digi}}},$$

$$\Gamma = (\Phi - I) A^{-1} B,$$

and

$$k_{d} = (\Phi - I) A^{-1} k$$

are the discretizations of $A, B$ and $k$, respectively, obtained by the ZOH method [51].

Note that, in contrast to other state estimators, e.g., the Kalman filter approach proposed in [15], knowing the sign of the estimation error $e_{1,m}$ is sufficient for the SMO. Hence, fewer multiplications are necessary for updating the state estimate, and the SMO can be implemented with low computational complexity in the digital domain.

### 4.2 Current Reconstruction Limitations

Before providing simulation results of the proposed SMO, some of its limitations and of state estimation for multi-phase converters in general are discussed in the following paragraphs.
From control theory, it is well-known that in order for the system states to be observable from output measurements alone, the so-called observability matrix

$$M_{\text{obs}} = \begin{bmatrix} C \\ CA \\ \vdots \\ CA^O \end{bmatrix}, \quad (4.19)$$

with the system matrix $A$, the output matrix $C$ and the system order $O$, is required to have full rank. For the $N$-phase buck converter topology considered in this work, $O = (N + 1)$, with the state vector as defined in (3.2). Furthermore, the output matrix $C$ reduces to the row vector

$$c^T = [1 \ 0 \ \cdots \ 0] \quad (4.20)$$

if the output voltage $v_{\text{out}}(t)$ is the only measured state variable.

For a converter with identical phases, i.e., $R_{p1} = \cdots = R_{pN}$, and $L_1 = \cdots = L_N$, it can be easily shown that $M_{\text{obs}}$ does not have full rank if the output matrix is given by (4.20), i.e., only $v_{\text{out}}(t)$ is measured. Consequently, the system is not observable. As already discussed in Section 2.2, in a real-world SMPS, not all phases are equal. Nevertheless, the exact values of these mismatches, e.g., the parasitic resistances, are typically not known. Therefore, a state estimator, e.g., the SMO introduced in this chapter, calculates its estimate based on the nominal system and input matrices $A$ and $B$, respectively. Since this system is not observable, it follows, in principle, that the individual inductor currents cannot be estimated by an output voltage measurement alone.

This fact can be intuitively understood by considering a two-phase buck converter, as it is used throughout this work. Assume, without loss of generality, that the parasitic resistance of the second phase is larger than that of the first one, i.e., $R_{p2} > R_{p1}$. Furthermore, a common duty cycle $d(t)$ is applied to both phases. As has been outlined in Section 2.2.3, the first phase then provides more current to the load, since the phase current ratio is inversely proportional to the ratio of the parasitic resistances [42]. This current imbalance is not reflected in the output voltage. In other words, the same output voltage would be observed if $R_{p1} > R_{p2}$ or $R_{p1} = R_{p2}$. Therefore, it is not possible to employ a state observer in order to remove the current imbalance between the phases.

Nevertheless, as will be supported by both simulation and measurements results, the proposed SMO can be used to estimate the AC components of the inductor current and no additional compensation, as described in [26], [62], [96], is required for preventing the drift of the inductor currents.
4.3 Simulation Results

To verify the presented observer, simulations for a two-phase buck converter with the control approach introduced in Chapter 3 have been carried out. In order to facilitate a fair comparison with a controller that employs current sensing, the same converter and controller parameters as reported in Section 3.4 have been selected. Furthermore, for the SMO design, \( k_1 = 2.5 \times 10^5 \), \( Q = I \), and \( R = 1 \), which yield an observer bandwidth of \( \omega_{SMC} = 2\pi \cdot 11 \text{kHz} \) and a damping factor \( \zeta_{SMO} = 1 \), were selected.

In Figure 4.1a, the output voltage transient response to a load release from 2 A to 0 A followed by a load jump back to 2 A is reported. A controller with perfect state knowledge (denoted as SMC) serves as a reference. Virtually, the same dynamic performance as with current measurement is achieved with the proposed SMO. In Figure 4.1b, the phase currents \( i_{L_1}(t) \) and \( i_{L_2}(t) \), as well as their estimates \( \hat{i}_{L_1,m} \) and \( \hat{i}_{L_2,m} \) obtained with the SMO, are reported. Note that, the actual phase currents are covered by their estimates, which underlines the estimation accuracy of the SMO. For this simulation, the nominal plant parameters have been selected. Hence, both phases are identical and the SMO uses the exact DT model of the plant. Consequently, not only the high frequency content of the phase currents can be estimated, but the DC components are also obtained.

The output voltage transient response to a sudden change of the input voltage from the nominal value of 3.3 V to 5 V and back to 3.3 V is depicted in Figure 4.2a. As can be seen, the controller with perfect state knowledge exhibits the smallest undershoot and fastest settling time. A similar performance is also observed if the proposed SMO is employed. Even if no input voltage information is available in the observer and a static value \( v_{in,m} = 3.3 \text{V} \) is programmed (denoted as SMC & SMO w/o \( v_{in,m} \) feed-forward), the controller still achieves regulation, although the dynamic performance degrades. In Figure 4.2b, the inductor current transient for the SMO with a programmed constant input voltage is depicted. Clearly, the SMO is not able to estimate the inductor currents correctly, since a wrong value for the input voltage is used. This explains the longer settling times and larger under- and overshoots during line transients.

To investigate the effect of parameter variations on the SMO and in turn on the SMC, a mismatch between the phases has been introduced deliberately. More specifically, \( L_2 \) has been decreased by 30\%, i.e., \( L_2 = 2.31 \text{μH} \), and \( R_p \) has been changed from 220 m\( \Omega \) to 100 m\( \Omega \). Note that, these changes have only been performed for the converter model used in the simulation, whereas the system and input matrices of the SMO have been left unchanged. As reported in Figure 4.3a, the dynamic behavior changes but regulation and stability is still maintained. To be more precise, in this case, the under- and overshoots are
Figure 4.1: Load jump from 2 A to 0 A and back for a sliding mode controlled two-phase buck converter. The transient response of the controller with the proposed SMO for digital current reconstruction is compared to a response obtained by a controller with current measurement.
Figure 4.2: Line jump from 3.3 V to 5 A and back for a sliding mode controlled two-phase buck converter. The transient response of the controller with the proposed SMO for digital current reconstruction is compared to a response obtained by a controller with current measurement.
reduced in comparison to the controller with current measurement. This is expected, since the SMC and SMO were designed for the nominal plant with a larger $L_2$, i.e., a slower system. Without the SMO, this mismatch is compensated by the current measurement, which provides the real slope of the phase currents. In contrast to that, the slope of the current estimate $\hat{i}_{L,2,m}$, as shown in Figure 4.3b, is too small. In order to obtain the same controller bandwidth, the controller coefficients grow with increasing inductor size. Therefore, the gains of the nominal controller are larger than the ones that would be required for a plant with a smaller $L_2$. Consequently, the controller overreacts, yielding the reduced over- and undershoots. In other words, the controller bandwidth is unintentionally increased, resulting in a faster dynamic response. Note that, it is not possible to increase the bandwidth arbitrarily, since the stability is decreased at the same time. Hence, it is important to design the controller in such a way that it is stable over all possible $L$ and $C$ variations, which typically sacrifices performance. In Chapter 5, controller auto-tuning methods based on SI are proposed. These techniques simplify the design procedure by automatically adapting the controller coefficients to the actual converter parameters.

Moreover, Figure 4.3b confirms the discussion in Section 4.2. As concluded therein, the DC components of the phase currents cannot be observed in the case of unknown parameter variations and mismatches. Nevertheless, no drift of the estimates $\hat{i}_{L,1,m}$ and $\hat{i}_{L,2,m}$ occurs, even with such large parameter differences between the plant and the ones used by the observer.
Figure 4.3: Load jump from 2 A to 0 A and back for a sliding mode controlled two-phase buck converter. The actual converter parameters \( L_2 \) and \( R_p \) have been set to 2.31 \( \mu \)H and 100 m\( \Omega \), respectively, whereas the SMO uses the nominal parameters.
As already discussed, a control system for an SMPS is often designed for the worst case plant parameters. In order to improve the performance and maintain stability under time-varying operating conditions and for different component sets, SI can be employed.

This chapter introduces different SI approaches for SMPSs. Firstly, a state-space-based parametric SI is proposed. In contrast to typical approaches, which only estimate the duty cycle to output voltage TF, the presented method yields a model of the converter in the DT state-space. Therefore, auto-tuning of more sophisticated control structures than a standard PID controller is straightforward. Exemplarily, an FSF controller is employed in this work. The proposed state-space estimation approach reduces the computational complexity in comparison to TF methods, since fewer parameters have to be estimated. Moreover, an improved estimation accuracy can be achieved with the same number of iterations. The faster convergence speed, reduced complexity, and improved accuracy of the proposed approach compared to the state of the art are later demonstrated on the example of a two-phase buck converter.

Secondly, an SI method especially designed for SMC is proposed. By reformulating the sliding surface calculation, the previously introduced estimation algorithm can be adapted in order to be used with this non-linear control approach. Additionally, a small-signal TF model of the closed-loop system, including a digital current reconstruction, is derived and a simple controller tuning method is presented.

Finally, a natural frequency estimation scheme with a very low computational complexity is introduced. This approach fundamentally differs from the state of the art. In contrast to typical SI methods for SMPSs, it is not necessary to measure the output voltage with a relatively high resolution ADC. Rather, it is sufficient to detect the transitions of the switching node voltage, for which a simple comparator can be employed.

5.1 STATE-SPACE-BASED SYSTEM IDENTIFICATION

Parametric SI approaches generally require a system model, whose parameters are then estimated. Therefore, for validation purposes, it is beneficial to derive a suitable model of the system to be estimated in advance. Since the converter model and the controller structure
have already been introduced in Section 2.2.3 and Section 2.2.4, respectively, only a brief summary is given in this section.

5.1.1 System model

Following the approach outlined in Section 2.2.3, a CT state-space model of an N-phase buck converter can be derived:

\[
\dot{x}(t) = Ax(t) + Bv(t)
\]  

\[
y(t) = Cx(t).
\]  

Here, \( A \in \mathbb{R}^{2 \times 2} \) is the system matrix, \( B \in \mathbb{R}^{2 \times 2} \) is the input matrix, \( C \in \mathbb{R}^{2 \times 2} \) is the output matrix, the state vector is given by \( x(t) = [v_{\text{out}}(t) \ i_L(t) = i_{L_1}(t) + \cdots + i_{L_N}(t)]^T \), the input vector is \( v(t) = [(c_1(t) + \cdots + c_N(t)) \cdot v_{\text{in}}(t) \ i_i(t)]^T \), and the output vector is \( y(t) = [v_{\text{out}}(t) \ i_L(t)]^T \). In order to facilitate the derivation of this model, it has been assumed that \( L_1 = \cdots = L_N \) and \( R_{p_1} = \cdots = R_{p_N} \) hold. Typically, the individual power stages of a multi-phase converter are designed to be equal in order to fully exploit the benefits, e.g., switching ripple reduction, of this topology [9]. Hence, these simplifications are reasonable. By introducing \( i_L(t) \) as a state variable instead of the individual phase currents, the number of parameters that have to be estimated is reduced, which in turn results in a lower computational complexity. In addition, this number, and hence the proposed SI scheme, is independent of the number of employed phases. This explains the simplifications made in (5.1) with respect to the models derived in Section 2.2.3. By SSA and subsequent linearization, an LTI small-signal model given as [2]

\[
\dot{\hat{x}}(t) = A\hat{x}(t) + B \begin{bmatrix} V_{\text{in}} \\ 0 \end{bmatrix} \hat{d}(t),
\]  

\[
\hat{y}(t) = C\hat{x}(t),
\]  

is obtained. In (5.2a), the small-signal duty cycle \( \hat{d}(t) \) represents the new control input, and the steady state input voltage is given by \( V_{\text{in}} \). Furthermore, all small-signal quantities are marked by a tilde. It should be noted that, all phases use the same duty cycle as their control input in the small-signal model. Moreover, instead of each individual phase current, only the sum of the inductor currents represents a state variable. As will be shown later, this is fully justified for the presented controller, which calculates a common duty cycle for all phases.
The delays caused by the DPWM are also appropriately modeled. As depicted in Figure 2.12a, in the employed trailing-edge modulation scheme, the duty cycle is updated at the beginning of the first phase’s switching period. Hence, the DPWM delays of the phases can be approximated according to (2.67). Therefore, the overall output delay is given by $T_{d,\Sigma} = \frac{1}{N} \sum_{n=1}^{N} T_{d,n}$ [14].

Then, applying the impulse-invariant transform with sampling period $T_{sw}$ to (5.2), with the output delay $T_{d,\Sigma}$ considered, yields the DT converter model [47]

$$x_{k+1} = \Phi x_k + \gamma d_k,$$  \hspace{1cm} (5.3a)

$$y_k = C x_k.$$  \hspace{1cm} (5.3b)

The subscript $k$ denotes the $k^{th}$ switching period, and the DT system and input matrices are given by $\Phi$ and $\gamma$, respectively. As has been shown in Section 2.2.3, if the component values of the converter are exactly known, (5.3) represents an accurate DT model of the converter. This model can be used to design a digital FSF controller.

### 5.1.2 Controller

While an FSF has already been derived in Section 2.2.4, a modified version, with a single duty cycle for all phases, is illustrated in the following paragraphs. For the system model with a common duty cycle as control input, the augmented plant is governed by

$$\begin{bmatrix} x_{k+1} \\ x_{i,k+1} \\ x_{aug,k+1} \end{bmatrix} = \begin{bmatrix} \Phi & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} x_k \\ x_{i,k} \\ x_{aug,k} \end{bmatrix}$$  
$$+ \begin{bmatrix} \gamma \\ 0 \\ 0 \end{bmatrix} d_{c,k} + \begin{bmatrix} 0 \\ 0 \\ V_{ref} \end{bmatrix} \delta_{aug}.$$  \hspace{1cm} (5.4)

The duty cycle $d_{c,k}$, which is calculated by the controller, satisfies the equation

$$d_{c,k} = -k x_{aug,k},$$  \hspace{1cm} (5.5)

with the gain vector $k$ and the update of the integrator state $x_{i,k}$ computed as

$$x_{i,k+1} = x_{i,k} + (V_{ref} - v_{out,k}).$$  \hspace{1cm} (5.6)
Substituting the RHS of (5.5) for $d_k$ in (5.4), yields the closed-loop system

$$x_{\text{aug}, k+1} = \Phi_{\text{aug}} x_{\text{aug}, k} - \gamma_{\text{aug}} k x_{\text{aug}, k} + \delta_{\text{aug}}$$

$$= \underbrace{\left( \Phi_{\text{aug}} - \gamma_{\text{aug}} k \right)}_{\Phi_{\text{cl}}} x_{\text{aug}, k} + \delta_{\text{aug}}. \quad (5.7)$$

Here, $\Phi_{\text{cl}}$ denotes the closed-loop system matrix, which determines the dynamic response and stability of the plant with the FSF controller. The required gain vector $k$ for the desired closed-loop dynamics, i.e., bandwidth and damping factor, is readily obtained by pole placement [51]. Note that, although (5.5) includes the summed inductor currents $i_{L,k}$, current sensing is actually not necessary. Instead, a current observer, such as the SMO proposed in Chapter 4, can be used to obtain a current estimate $\hat{i}_{L,k}$.

### 5.1.3 System identification concept

As outlined in the previous section, the state-space model allows for a straightforward controller design if $\Phi$ and $\gamma$ are precisely known. Model limitations and other uncertainties, e.g., component tolerances, introduce mismatches between the converter model and the actual SMPS. Depending on the choice of $k$, these mismatches may result in instabilities or degraded performance of the implemented controller. Therefore, SI can be employed to obtain accurate estimates $\hat{\Phi}$ and $\hat{\gamma}$ of the real converter’s system and input matrix, respectively. Consequently, these estimates can then be used to automatically tune the controller accordingly, yielding an improved performance. It should be noted that, in the proposed scheme, the parameters of the converter, e.g., $L_n$ and $C$, are not estimated. Rather, as outlined above, the coefficients of the system matrix $\Phi$ and the input matrix $\gamma$ of a DT system, which models the converter, are to be estimated.

Figure 5.1 illustrates the proposed SI concept. The duty cycle $d_{c,k}$ is calculated by the controller according to (5.5), whereby the current estimate $\hat{i}_{L,k}$ is obtained by a current observer. During SI, the stimulus $d_{p,k}$ is superimposed on the duty cycle $d_{c,k}$. The output voltage $v_{\text{out}, k}$, current observer output $\hat{i}_{L,k}$, and duty cycle $d_k$ samples obtained during SI are stored until the stimulus injection is finished. Then, the measurement matrix $Y = \begin{bmatrix} v_{\text{out}} & \hat{i}_{L} \end{bmatrix} \in \mathbb{R}^{(M-1)\times 2}$ and the observation matrix $H \in \mathbb{R}^{(M-1)\times 3}$ are composed, with $M$ denoting the perturbation length in number of switching periods. The $(k+1)^{\text{th}}$ row $h_{(k+1)^T} = \begin{bmatrix} v_{\text{out}, k} & \hat{i}_{L,k} & d_k \end{bmatrix}$ of $H$ contains the delayed input and output samples. In the next step, with $Y$ and $H$ available, the randomized SALS (R-SALS) algorithm iteratively calculates $\hat{\Theta}$, which contains the estimates of $\Phi$ and $\gamma$. Finally, utilizing these estimated system pa-
rameters, the controller coefficients are accordingly tuned, such that the target specification is met.

One of the most critical factors in terms of computational complexity is the number of parameters $P$ that have to be estimated. For the converter model (5.3), $P = 6$, since $\Phi \in \mathbb{R}^{2 \times 2}$ and $\gamma \in \mathbb{R}^{2 \times 1}$. Note that, in a TF estimation approach, $P = 8$ parameters have to be estimated, since $z$-transforming (5.3) yields two second-order TFs, each with two poles and zeros [47]. Hence, the overall complexity is reduced by employing the proposed state-space-based approach. Furthermore, as will be shown by measurements in Section 7.3.1, convergence speed and accuracy are improved in comparison with a $z$-domain estimation approach.

5.1.3.1 Stimulus

For the estimation process, as in other SI approaches, the system has to be perturbed by some kind of excitation signal. Typically, broadband signals, such as a random sequence or a chirp signal are selected as stimulus [72], [73]. From a computational complexity point of view, one of the most attractive excitation signals is a PRBS. Such a sequence of only two distinct values and of length $M$ can be easily obtained by a linear-feedback-shift register (LFSR) with $\log_2 (M + 1)$ taps. Despite its simple generation procedure, a PRBS exhibits desirable properties for identification purposes such as a flat power spectrum [97]. In this work, an LFSR operated at the switching frequency $f_{sw}$ is employed in order to generate the PRBS. To obtain the specified magnitude of the
perturbation $d_{p,k}$, the output of the LFSR is then scaled accordingly. Note that, the amplitude of $d_{p,k}$ is a design parameter. Larger magnitudes of $d_{p,k}$ typically improve the estimation accuracy and speed, while simultaneously increasing the perturbation of the output voltage and inductor currents. Hence, the amplitude choice depends on various parameters such as tolerable output voltage deviation, stimulus injection time, noise level and ADC resolution.

5.1.3.2 Estimation Algorithm

With the output matrix $Y$ and the observation matrix $H$ available, the relationship between the outputs of the system and its inputs can be written in linear form as

$$Y = H \begin{bmatrix} \Phi & \gamma \end{bmatrix}^T + N. \quad (5.8)$$

Here, the measurement noise is combined in the matrix $N$. Note that, (5.8) typically has no exact solution, since $M > P$, i.e., the system of equations is overdetermined, and the measurements are furthermore corrupted by noise. Instead, the LLS solution of (5.8) is obtained by minimizing the cost function

$$J(\Theta) = \text{tr} \left( (Y - H\Theta)^T (Y - H\Theta) \right). \quad (5.9)$$

In other words, the minimization of (5.9) yields the parameter matrix estimate $\hat{\Theta} = \begin{bmatrix} \hat{\Phi} & \hat{\gamma} \end{bmatrix}^T$ comprising the estimates $\hat{\Phi}$ and $\hat{\gamma}$ of the system matrix $\Phi$ and input matrix $\gamma$, respectively. As indicated by (5.9), the LLS solution minimizes the sum of the squared residuals. This estimation scheme is optimal in the sense that it yields the solution with the minimum sum of squared errors. Note that, conventional LLS as reviewed in Section 2.4.1, estimates a parameter vector $\theta$. In contrast to that, for the state-space SI approach proposed in this work, the objective is to find an estimate of a matrix $\Theta$. Therefore, the trace operator $\text{tr} (\cdot)$ is used in (5.9) to obtain a scalar cost function. Although the analytical solution to (5.9) can be calculated as

$$\hat{\Theta} = \left( H^T H \right)^{-1} H^T Y, \quad (5.10)$$

the involved multiplications and matrix inversion pose a significant challenge for many applications due to their high computational complexity and numerical precision requirements [88]. Hence, the objective of the SALS estimation algorithm proposed in this work is to approximate the exact solution of (5.9) with low computational complexity. In each iteration $n$ of the SALS algorithm, an update [86]

$$\Theta^{(n)} = \hat{\Theta}^{(n-1)} + \mu^{(n)} h_i \left[ \frac{y_i^T - h_i^T \hat{\Theta}^{(n-1)}}{e^{(n)}} \right], \quad (5.11)$$
of the parameter matrix estimate is calculated. In (5.11), $h_i^T$ and $y_l^T$ denote the $l$th row of $H$ and $Y$, respectively. Before explaining the selection strategy for $l$, the calculation of the step size $\mu^{(n)}$ is discussed in more detail.\footnote{Note that, $l$ also depends on the iteration step $n$, i.e., $l(n)$ would be the more precise notation. Nevertheless, this dependency on $n$ is not explicitly indicated in order to improve readability.} In this work, a dynamic step size calculated by $\mu^{(n)} = \frac{1}{\|h_l^T\|^2_2}$ is used, which improves convergence speed in comparison with a constant step size. Furthermore, if the error $e^{(n)}$ does not decrease significantly anymore, $\mu^{(n)}$ can be reduced in the subsequent iteration steps. When reducing the step size, a further error reduction can then be achieved, and hence, the estimation accuracy is improved. A way to perform such a reduction is the following approach. If $\|e^{(n)}\|_2 - \|e^{(n-1)}\|_2 < e_{th}$ in the $n_r$th iteration, the step size is first set to the value $\mu^{(n_r)} = \frac{1}{\max_{m=1,\ldots,M-1} \|h_m^T\|^2_2}$.

Here, $e_{th}$ defines a threshold value for the step size reduction. In the remaining iterations, $\mu^{(n)}$ is then calculated as $\mu^{(n)} = \mu^{(n-1)} - \mu_r$ with $\mu_r = \frac{\mu^{(n_r)}}{N-n_r+1}$. Note that, $\mu_r$ is only calculated once, with $n_r$ being the iteration step where $\|e^{(n)}\|_2 - \|e^{(n-1)}\|_2 < e_{th}$ first holds. This approach has a very low computational complexity: when calculating the update of $\mu^{(n)}$ it requires only a subtraction at every iteration.

In contrast to incrementing the row index $l$ in each iteration step, $l$ is randomly selected using the selection strategy of the Randomized Kaczmarz algorithm \cite{87, 98}, yielding the R-SALS algorithm. For this selection, a cumulative sum $F(m) = \sum_{j=1}^{m} \frac{\|h_l^T\|^2_2}{\sum_{i=1}^{M-1} \|h_i^T\|^2_2}$ $\forall m \in \{1, 2, \ldots, M-1\}$ is calculated once, before the first iteration step. Then, the row index $l$ in the $n$th iteration step is selected such that $F(l-1) \leq r^{(n)}$ and $F(l+1) \geq r^{(n)}$ are fulfilled, using a uniformly distributed random
number $r^{(n)}$. This results in a selection probability for the rows of $H$ that is proportional to their squared norm. As outlined in [87], this further accelerates the convergence of the estimation. Algorithm 1 lists the complete R-SALS estimation algorithm. Further details about the actual hardware implementation are presented in Section 6.6.1, and measurement results are reported in Section 7.3.1.

Algorithm 1 R-SALS

1: define $e_{th}$, $n_{th}$
2: calculate $\mu_m = \frac{1}{||h_m||^2}$, $F(m)$ (5.16) $\forall m \in \{1, \ldots, M-1\}$
3: $\hat{\Theta}^{(0)} \leftarrow 0$, $e^{(0)} \leftarrow \infty$
4: ReduceMu $\leftarrow$ False
5: for $n = 1, \ldots, N$ do
6: $r^{(n)} \leftarrow \{\text{random number from } (0,1)\}$
7: $l \leftarrow \{l \mid F(l-1) \leq r^{(n)}, F(l+1) \geq r^{(n)}\}$
8: $e^{(n)} \leftarrow y_l^T - h_l^T \hat{\Theta}^{(n-1)}$
9: if ReduceMu then
10: $\mu^{(n)} \leftarrow \mu^{(n-1)} - \mu_r$
11: else
12: $\mu^{(n)} \leftarrow \mu_l$
13: if $n \geq n_{th}$ then
14: if $\left|\left|e^{(n)}\right|\right|_2 - \left|\left|e^{(n-1)}\right|\right|_2 < e_{th}$ then
15: $\mu^{(n)} \leftarrow \max_{m=1,\ldots,M-1} \mu_m$
16: $\mu_r \leftarrow \frac{\mu^{(n)}}{N-n+1}$
17: end if
18: end if
19: end if
20: $\hat{\Theta}^{(n)} \leftarrow \hat{\Theta}^{(n-1)} + \mu^{(n)} h_l e^{(n)}$
21: end for

5.1.3.3 Controller Tuning

After $N$ iterations, the estimator output $\hat{\Theta} = \begin{bmatrix} \hat{\phi}^N & \hat{\gamma}^N \end{bmatrix}^T$ is selected as the converter model parameters. Here, $N$ can either be dynamically determined based on the estimation error $e_n$ or set to a preselected constant. This work follows the latter approach, in order to always ensure the same run-time of the estimation algorithm.

Note that, $\hat{\Theta}^N$ contains estimates of the converter’s discrete-time system matrix $\Phi$ and input vector $\gamma$. As already outlined in Section 5.1.2, with the model parameters identified, the design of an FSF controller can be carried out easily. In order to tune the controller for
the identified system, \( \Phi \) and \( \gamma \) in \((5.4)\) are substituted by \( \hat{\Phi}^N \) and \( \hat{\gamma}^N \), respectively, which yields the estimated closed-loop system matrix

\[
\hat{\Phi}_{cl} = \left( \hat{\Phi}^N_{aug} - \hat{\gamma}^N_{aug} k_t \right).
\] (5.17)

In \((5.17)\), \( k_t \) denotes the gain vector to be tuned for the estimated system. The tuning is carried out by placing the poles of \( \hat{\Phi}_{cl} \) at specified locations. To be more precise, the characteristic polynomial

\[
\Delta_{\hat{\Phi}_{cl}} = \det (zI - \hat{\Phi}_{cl})
\] (5.18)

of \( \hat{\Phi}_{cl} \) is set equal to the desired polynomial

\[
z^3 + a_{d,2}z^2 + a_{d,1}z + a_{d,0},
\] (5.19)

which describes the specified closed-loop dynamics according to the design parameters \( a_{d,2} \), \( a_{d,1} \), and \( a_{d,0} \). Note that, this essentially boils down to calculating the solution of a linear system of equations, consisting of three equations with three unknowns, whereby the elements of \( k_t \) represent the unknowns. As the R-SALS algorithm basically approximates such a solution [99], it can also be used for controller tuning. This is especially attractive in a hardware implementation, since the SI architecture can be reused for the task of controller tuning. Thus, computational complexity does not increase.

In Section 7.3.1, measurement results that highlight the convergence speed and accuracy of the proposed SI concept are reported. Furthermore, the achievable performance gain of the suggested auto-tuning approach is demonstrated.

5.2 SYSTEM IDENTIFICATION FOR SLIDING MODE CONTROL

In contrast to linear control schemes, SMC exhibits a higher robustness in the presence of parameter variations. Nevertheless, caused by the constant switching frequency implementation, and the requirement to support different output filter configurations, i.e., \( L \) and \( C \) pairs, the achievable dynamic performance of a controller with fixed gain coefficients might be reduced. Therefore, SI still presents an attractive solution for improving the performance of the SMPS. In this section, a modification of the SI approach with the low-complexity R-SALS at its core is suggested, which allows its usage in conjunction with a sliding mode controller, e.g., the one proposed in Chapter 3.

5.2.1 System model

With the direct implementation of the control law introduced in Chapter 3, implementing a parametric SI approach is not straightforward, since a stimulus injection is not simply possible and a suitable control-to-output TF or state-space model is not available. Hence, a different form of the control law is proposed. As illustrated in Figure 5.2,
it is possible to rewrite the turn on and off decisions $c^{\pm}$ in such a way that the sum $(\pm h_k - \hat{i}_{L_{n,m}})$ is compared to the new control input $v_{c,n,m} := (g_{d1}x_{1,m} + g_{d3}x_{3,m})$. Utilizing these rearranged switching decisions, one can split the control law into two parts. Firstly, a PI controller calculating $v_{c,m}$ from the sampled output voltage $v_{out,m}$ and the reference voltage $V_{ref}$ and secondly, the DPWM block generating the control command $c_{n,m}$ by comparing $v_{c,k}$ to the estimated inductor current and the hysteresis value. As described in Section 3.2, the SMC design procedure then reduces to selecting the coefficients $g_{d1}$ and $g_{d3}$, which represent the proportional and integral part of a PI controller. As already elaborated in Section 5.1, a fixed order model, which determines the number of parameters to be estimated, has to be selected in a parametric SI approach. If an analytically derived model of the system to be identified is available, it can be used to determine the model order and structure required for estimation. Furthermore, the SI results can then be verified more easily by comparing them to the analytical model. In Section 2.2.3, small-signal state-space models of a duty cycle controlled converter have been already derived. For SMC, which does not directly calculate a duty cycle, these models have to be extended in order to model the output voltage dynamics with respect to the new control input $v_{c,m}$.

Based on geometric observation, one is able to derive a state-space model describing the relationship between the small-signal components $\tilde{v}_{c,m}$ and $\tilde{v}_{out,m}$ of the control signal and the output voltage, respectively. To that end, the estimated inductor current $\hat{i}_{L,(k+1)}$ at the beginning of the $(k+1)^{th}$ switching period is expressed as

$$\hat{i}_{L,(k+1)} = \hat{i}_{L,k} + \dot{i}_{L,k}T_{on,k} - \dot{i}_{L,k}T_{off,k}.$$  

(5.20)
As anticipated by Figure 5.2,
\[ \dot{\sigma}_k^+ = \frac{v_{in,k} - v_{out,k} - \dot{i}_{L,k}R_p}{L} \]  
(5.21)
and
\[ \dot{\sigma}_k^- = \frac{v_{out,k} + \dot{i}_{L,k}R_p}{L} \]  
(5.22)

denote the slopes of \( \dot{i}_{L,m} \) during the on-time \( T_{on,k} \) and the off-time \( T_{off,k} \) respectively, which can be obtained from (4.15). Similar to the derivation of the hysteresis control TFs in Section 3.3, (5.21) and (5.22) are required to be constant during the \( k \)th switching period. With the observer proposed in Chapter 4, this can be simply achieved by updating \( v_{in,k} \) and \( v_{out,k} \) only at the beginning of a switching period. Moreover, a constant switching period length \( T_{sw} \) is assumed, which is a result of the frequency control loop proposed in Section 3.3. Therefore, as analyzed in Section 3.3, \( T_{on,k} \) is given by
\[ T_{on,k} = \frac{h_k - v_{c,k} - \dot{i}_{L,k}}{\dot{\sigma}_k^+}. \]  
(5.23)

In order to obtain an expression for \( T_{off,k} \), the peak value of the estimated inductor current, i.e., \( \dot{i}_L (kT_{sw} + T_{on,k}) \) is first derived. As Figure 5.2 shows, \( \dot{i}_L (kT_{sw} + T_{on,k}) \) and \( (h_k - v_{c,k}) \) are equal.\(^2\) Thus, substituting \( (h_k - v_{c,k}) \) in (5.23) with \( \dot{i}_L (kT_{sw} + T_{on,k}) \) and solving for it yields
\[ \dot{i}_L (kT_{sw} + T_{on,k}) = \dot{i}_{L,k} + \dot{\sigma}_k^+ T_{on,k}. \]  
(5.24)

By using another geometric argument one can see that \( \dot{i}_{L,(k+1)} = (-h_k - v_{c,k}) \) holds. From that,
\[ \dot{i}_L (kT_{sw} + T_{on,k}) = (-h_k - v_{c,k}) + \dot{\sigma}_k^- T_{off,k} \]  
(5.25)

immediately follows. Finally, by equating the RHSs of (5.24) and (5.25) with each other and solving for \( T_{off,k} \), one is in the position to express \( T_{off,k} \) as
\[ T_{off,k} = \frac{\dot{i}_{L,k} + \dot{\sigma}_k^+ T_{on,k} + h_k + v_{c,k}}{\dot{\sigma}_k^-.} \]  
(5.26)

In order to facilitate the derivations above, an update of \( v_{c,k} \) only once per switching cycle has been assumed. The reduced control delay if \( v_{c,k} \) is updated more often is addressed later by adapting the duty-cycle-to-output-voltage TF accordingly.

\(^2\) Note that, these quantities are digital signals inside the controller. Therefore, despite the different units, their addition does not pose any conceptual difficulty. Nevertheless, in order to be more precise, the coefficients of the gain matrix \( G_d \) are not dimensionless, thus ensuring the alignment of the units.
As a next step, (5.20) is linearized in order to obtain a linear representation of its small-signal component $\hat{i}_{L,k}$. Following the same general procedure as outlined in Section 2.2.3, differentiating (5.20) with respect to $\hat{i}_{L,k}$ and the inputs $v_{c,k}$, $h_k$, $v_{in,k}$, and $v_{out,k}$, yields the the linear small-signal difference equation

$$
\hat{z}_{i_{L,(k+1)}} = \left. \frac{\partial \hat{i}_{L,(k+1)}}{\partial i_{L,k}} \right|_Q \hat{z}_i + \left. \frac{\partial \hat{i}_{L,(k+1)}}{\partial v_{c,k}} \right|_Q \hat{v}_{c,k} + \left. \frac{\partial \hat{i}_{L,(k+1)}}{\partial h_k} \right|_Q \hat{h}_k + \left. \frac{\partial \hat{i}_{L,(k+1)}}{\partial v_{in,k}} \right|_Q \hat{v}_{in,k} + \left. \frac{\partial \hat{i}_{L,(k+1)}}{\partial v_{out,k}} \right|_Q \hat{v}_{out,k}
$$

(5.27)

with the operating point defined as

$$
Q := \begin{bmatrix} I_L & V_c & h & V_{in} & V_{out} \end{bmatrix}^T.
$$

(5.28)

Here, the steady state value of $h$ for the nominal switching period length $T_{sw}$ can be calculated according to (3.29). Furthermore, since $T_{on} = DT_{sw}$ during steady state, the constant control input $V_c$ can be derived from (5.23) as

$$
V_c = h - (DT_{sw} \phi_{ss}^+ + I_L),
$$

(5.29)

with $D$ as given in (2.30).

The duty cycle $d_k$ in the $k^{th}$ switching cycle can then be expressed as

$$
d_k = \frac{T_{on,k}}{T_{on,k} + T_{off,k}}.
$$

(5.30)

Hence, its small signal dynamics as a function of $\hat{i}_{L,k}$, $v_{c,k}$, $h_k$, $v_{in,k}$, and $v_{out,k}$ are obtained in a similar fashion as the derivation of $\hat{i}_{L,(k+1)}$ in (5.27), yielding

$$
d_k = \left. \frac{\partial d_k}{\partial i_{L,k}} \right|_Q \hat{z}_i + \left. \frac{\partial d_k}{\partial v_{c,k}} \right|_Q \hat{v}_{c,k} + \left. \frac{\partial d_k}{\partial h_k} \right|_Q \hat{h}_k + \left. \frac{\partial d_k}{\partial v_{in,k}} \right|_Q \hat{v}_{in,k} + \left. \frac{\partial d_k}{\partial v_{out,k}} \right|_Q \hat{v}_{out,k}.
$$

(5.31)

Then, by combining (5.27) and (5.31), a single small-signal state-space model of the form

$$
\hat{z}_{i_{L,(k+1)}} = \phi_{i_{L,k}} \hat{z} + \gamma^T \bar{u},
$$

(5.32a)
\[
\tilde{d}_k = \tilde{c}_{L,k} + e^T \tilde{u}
\]  
(5.32b)

with the components of \(h^T\) and \(e^T\) given by \(\gamma_{1,...,4}\) and \(e_{1,...,4}\), respectively, and \(\tilde{u}\) defined as

\[
\tilde{u} := \begin{bmatrix}
\tilde{\varphi}_{c,k} \\
\tilde{h}_k \\
\tilde{\varphi}_{in,k} \\
\tilde{\varphi}_{out,k}
\end{bmatrix}
\]  
(5.33)

is obtained.

For the sake of completeness, and since the hardware implementation presented in Section 6.6.1 follows such an approach, the small-signal model for an SR flip-flop SMC is also derived in the following. In Figure 5.3, the relevant waveforms of this control scheme are shown. In contrast to hysteresis SMC, a ramp signal with constant slope \(S_r\) is required in order to prevent subharmonic oscillations if the duty cycle becomes larger than 0.5, i.e., for \(D > 0.5\) [2]. Moreover, the switching decisions are redefined as

\[
c_{n,m} = \begin{cases}
 c_n^- := 0 & \text{if } \sigma_{n,m}(x_{c,m}) \geq 0 \\
 c_n^+ := 1 & \text{if } \text{CLK}_{n,m} = 1 \\
 c_{n,(m-1)} & \text{else}
\end{cases}
\]  
(5.34)

Here, \(\text{CLK}_{n,k}\) denotes an impulse train with period \(T_{sw}\) and delay \(\frac{(n-1)T_{sw}}{N}\). For this kind of modulation scheme, (5.20) also holds. Moreover, the slopes of \(\dot{i}_{L,k}\) during \(T_{on,k}\) and \(T_{off,k}\) are again given by (5.21) and (5.22), respectively. In contrast to that, the slope \(S_r\) of the artificial ramp signal has to be considered in order to calculate the on-time \(T_{on}\). As can be deduced from Figure 5.3, \(\dot{i}_L(kT_{sw} + T_{on,k})\) can be determined to be

\[
\dot{i}_L(kT_{sw} + T_{on,k}) = \dot{i}_{L,k} + \dot{\sigma}_k^+ T_{on,k} = v_{c,k} - S_r T_{on,k}
\]  
(5.35)

and from that,

\[
T_{on,k} = \frac{v_{c,k} - \dot{i}_{L,k}}{\dot{\sigma}_k^+ + S_r}
\]  
(5.36)

immediately follows. Furthermore,

\[
T_{off,k} = T_{sw} - T_{on,k}
\]  
(5.37)
which is a direct consequence from the definition of $T_{sw}$, holds. Thus, the linear small-signal model of $\hat{i}_{L,(k+1)}$ for this modulation scheme yields

$$
\ddot{\hat{i}}_{L,(k+1)} = \frac{\partial \hat{i}_{L,(k+1)}}{\partial \hat{i}_{L,k}} Q \ddot{\hat{i}}_{L,k} + \frac{\partial \hat{i}_{L,(k+1)}}{\partial \hat{v}_{c,k}} Q \ddot{\hat{v}}_{c,k} 
$$

$$
+ \frac{\partial \hat{i}_{L,(k+1)}}{\partial \hat{v}_{in,k}} Q \ddot{\hat{v}}_{in,k} + \frac{\partial \hat{i}_{L,(k+1)}}{\partial \hat{v}_{out,k}} Q \ddot{\hat{v}}_{out,k} \tag{5.38}
$$

with the operating point

$$
Q := \begin{bmatrix} I_L & V_c & V_{in} & V_{out} \end{bmatrix}^T. \tag{5.39}
$$

Note that, $V_c$ is not equal to the one derived for hysteresis SMC in (5.29). Rather, the steady state value of the control signal is obtained from (5.36) as

$$
V_c = DT_{sw} (\dot{\sigma}_{ss}^+ + S_r) + I_L. \tag{5.40}
$$

Furthermore, with the definition of $d_k$, i.e.,

$$
d_k = \frac{T_{on,k}}{T_{sw}}, \tag{5.41}
$$

the small signal dynamics of the duty cycle can be expressed as

$$
\ddot{d}_k = \frac{\partial d_k}{\partial \hat{i}_{L,k}} Q \ddot{\hat{i}}_{L,k} + \frac{\partial d_k}{\partial \hat{v}_{c,k}} Q \ddot{\hat{v}}_{c,k} 
$$

$$
+ \frac{\partial d_k}{\partial \hat{v}_{in,k}} Q \ddot{\hat{v}}_{in,k} + \frac{\partial d_k}{\partial \hat{v}_{out,k}} Q \ddot{\hat{v}}_{out,k}. \tag{5.42}
$$

In an analogous fashion as for the hysteresis SMC scheme, a small-signal state-space model

$$
\ddot{\hat{i}}_{L,(k+1)} = \phi \ddot{\hat{i}}_{L,k} + \gamma^T \ddot{\hat{u}}, \tag{5.43a}
$$

$$
\ddot{\hat{d}}_k = \ddot{\hat{i}}_{L,k} + e^T \ddot{\hat{u}} \tag{5.43b}
$$

with

$$
\ddot{\hat{u}} := \begin{bmatrix} \ddot{\hat{v}}_{c,k} \\ \ddot{\hat{v}}_{in,k} \\ \ddot{\hat{v}}_{out,k} \end{bmatrix}. \tag{5.44}
$$
is then readily obtained from (5.38) and (5.41).

In Figure 5.4, the small-signal block diagram of the closed-loop system is depicted. For the small-signal model, the control signal vector $c_m$ is replaced by the small-signal quantity $d_k$. Hence, the converter itself can be modeled by its small-signal state-space representation, as given by (2.73). Note that, the delay $T_d$ in (2.73) depends on the actual update rate of $v_{c,n,k}$ and can be calculated according to (2.67). As follows from Figure 5.4, the small-signal relationship between $v_{c,n,k}$ and $v_{out,k}$ for the hysteresis window (SR flip-flop) SMC implementation is obtained by a series connection of (5.32) ((5.43)) with (2.73) and subsequently closing the output voltage loop. Finally, this $(2N + 1)^{th}$ order system can be written as

$$
\dot{\mathbf{x}}_{cl,(k+1)} = 
\begin{bmatrix}
\dot{i}_{L_1,(k+1)} \\
\vdots \\
\dot{i}_{L_N,(k+1)} \\
\dot{v}_{C,(k+1)} \\
\dot{i}_{L_1,(k+1)} \\
\vdots \\
\dot{i}_{L_N,(k+1)}
\end{bmatrix} 
= \Phi_{cl} \mathbf{x}_{cl,k} + \Gamma_{cl} \mathbf{v}_{c,k}, 
$$

(5.45a)
Figure 5.4: Block level view of the converter with the SMC structure and the current observer.

\[ \hat{y}_k = C \tilde{x}_{cl,k}. \quad (5.45b) \]

With (5.45), an analytical model of a sliding mode controlled converter is available, which can be used for controller tuning and to verify the SI approach outlined in the next section.

5.2.2 System identification concept

The objective of the SI step is now to estimate the coefficients of the TF \( G_{v_c,v_{out}}(z) = \frac{v_{out}(z)}{v_c(z)} \) that is obtained by z-transforming (5.45). Consequently, using the estimate \( \hat{G}_{v_c,v_{out}}(z) \), the coefficients \( g_{d1} \) and \( g_{d3} \) of the gain matrix \( G_d \) can be tuned to obtain the specified dynamic performance. In Figure 5.5, the proposed SI concept for SMC is reported. During SI, a perturbation sequence \( v_{p,k} \) is superimposed onto the controller output \( v_{c,m} \) for a duration of \( M \) switching periods. As for the state-space-based approach discussed in Section 5.1, by choosing a PRBS as the perturbation signal, an efficient implementation with an LFSR is possible. After the stimulus injection is finished, the measurement vector \( y = v_{out,k} \in \mathbb{R}^{M \times 1} \) and observation matrix \( H \in \mathbb{R}^{M \times P} \) are compiled from the stored data. As in the previous section, \( P \) specifies the number of parameters to be estimated whereas \( H \) now contains the delayed samples of \( v_{out,k} \) and \( v_{c,k} \). While the analytical derivation of the control-to-output TF yields a third order system for \( G_{v_c,v_{out}}(z) \), it is proposed to use the two pole, one zero model

\[ \hat{G}_{v_c,v_{out}}(z) = \frac{\hat{b}_1 z + \hat{b}_0}{z^2 + \hat{a}_1 z + \hat{a}_0} \quad (5.46) \]

for SI. Therefore, four parameters \( (P = 4) \) have to be estimated. This reduces the estimation effort while achieving sufficient accuracy, as will be shown in Section 7.3.2.

With the measurement vector and observation matrix, the parameter vector estimate

\[ \hat{\theta} := \begin{bmatrix} \hat{b}_1 & \hat{b}_0 & \hat{a}_1 & \hat{a}_0 \end{bmatrix}^T \quad (5.47) \]
is readily calculated by the actual R-SALS algorithm listed in Algorithm 1. Finally, utilizing the identified system, the controller coefficients are tuned accordingly in order to achieve the desired closed-loop system response.

### 5.2.2.1 Controller tuning

As for the state-space controller, the estimator output $\hat{\theta}^{(N)}$ after $N$ iterations is used for determining $\hat{G}_{v_c,v_{out}}(z)$. With an estimate of the control-to-output TF available, it is now straightforward to tune the coefficients $g_{d1}$ and $g_{d3}$ of the sliding function (3.21) by pole placement. To that end,

$$
\begin{bmatrix}
\hat{b}_1 \\
\hat{b}_0 - \hat{b}_1 \\
-\hat{b}_0
\end{bmatrix}
\begin{bmatrix}
g_{d1} \\
g_{d3}
\end{bmatrix} =
\begin{bmatrix}
a_{d2} - \hat{a}_1 + 1 \\
a_{d1} + \hat{a}_1 - \hat{a}_0 \\
a_{d0} + \hat{a}_0
\end{bmatrix},
$$

(5.48)

with the coefficients of the desired closed-loop denominator polynomial given as $a_{d,\{0,...,3\}}$, has to be solved for $g_{d1}$ and $g_{d3}$. This task can again be accomplished by the R-SALS algorithm, which is especially attractive for an implementation in hardware, since it facilitates reusing the SI estimator.

The measurement results reported in Section 7.3.2 highlight the effectiveness of the proposed tuning approach. Furthermore, the accuracy of the suggested small-signal model is verified.
In this section, a novel method for estimating the SMPS’s natural frequency is proposed. In contrast to the other SI methods introduced in this work and the state of the art, no computationally complex operations, e.g., multiplications are required. Furthermore, a high resolution ADC for measuring the output voltage perturbation is not required. Instead, the mismatch between the on-time of the control signal and the effective on-time at the switching node is exploited. This mismatch is caused by the parasitic drain-source (DS) capacitances and the parasitic BDs of the power MOSFETs. As will be shown, it is not necessary that the value of the parasitic capacitance is known nor is it required to stay constant, e.g., over temperature. For simplicity, the proposed concept is explained on the example of a single-phase buck converter, but can be directly applied to different topologies and multi-phase converters. Subsequently, the estimated natural frequency can be used to tune a digital controller to improve the system’s dynamic performance. A tuning procedure that focuses on low computationally complexity is also outlined in this section.

5.3.1 System model

In order to explain the proposed SI concept, some parasitics and their implications on the converter’s behavior must be addressed. Up to now, these parasitics have not been considered, since their impact on the small-signal modelling process and controller design are negligible. However, they are essential for the SI approach introduced in the following and its understanding. In Figure 5.6 the schematic of a synchronous buck converter is reported. In contrast to the schematic shown in Figure 2.8, Figure 5.6 depicts the parasitic DS capacitances $C_{DS,1}$ and $C_{DS,2}$ of the HS and LS switches $Q_1$ and $Q_2$. Note that, although a PMOS is employed as a HS switch $Q_1$, the presented con-
5.3 Low-Complexity Natural Frequency Estimation

In Figure 5.7a, the steady state inductor current waveforms $i_{L,1}(t)$, $i_{L,2}(t)$, and $i_{L,3}(t)$ during a switching period for three different load currents, denoted as $i_{l,1}(t)$, $i_{l,2}(t)$, and $i_{l,3}(t)$, are shown. For small load currents, such as $i_{l,2}(t)$ and $i_{l,3}(t)$ in Figure 5.7a, a negative inductor current can be observed during a fraction of the switching period $T_{sw}$.
The control signal $c(t)$ and the switching node voltages $v_{sw,1}(t)$, $v_{sw,2}(t)$ and $v_{sw,3}(t)$, corresponding to the inductor current waveforms of Figure 5.7a, are depicted in Figure 5.7b. At the rising edge of $c(t)$, the LS switch $Q_2$ is turned off, while the HS switch $Q_1$ is still kept off for the dead-time duration $T_p$. Depending on the sign of $i_L(t)$ during $T_p$, two cases, namely

1. $i_L(t) \geq 0$
2. $i_L(t) < 0$

have to be considered [100].

**Case 1:** $i_L(t) \geq 0$

If $i_L(t)$ is positive during $T_p$, e.g., $i_{L,1}(t)$ in Figure 5.7a, the BD of $Q_2$ starts to conduct, since the potential at $v_{sw}(t)$ is negative, as shown by $v_{sw,1}(t)$.

The delayed turn on of $Q_1$ causes a mismatch $\Delta T_{on,1} := T_{on} - T_{on,sw,1}$, equal to $T_p$, between the steady state on-times $T_{on}$ and $T_{on,sw,1}$ of $c(t)$ and $v_{sw,1}(t)$, respectively. Here, the on-time $T_{on,sw,1}$ is defined as the timespan between $v_{sw,1}(t)$ exceeding a specified threshold $V_{th}$ and falling below this threshold. In this example, $V_{th}$, which is a design parameter in the proposed SI approach, is arbitrarily chosen to be $\frac{2}{3}V_{in}$, with $V_{in}$ representing the steady state input voltage.

**Case 2:** $i_L(t) < 0$

If the coil current $i_L(t)$ is negative at the beginning of the switching period, as is true for $i_{L,2}(t)$ and $i_{L,3}(t)$ in Figure 5.7a, the BD of $Q_2$ does not start to conduct. Instead, caused by the reverse direction of the current $i_L(t)$, the parasitic $DS$ capacitances of $Q_1$ and $Q_2$ are charged. Consequently, the potential of the switching node $v_{sw}(t)$ gradually increases as depicted by $v_{sw,2}(t)$ and $v_{sw,3}(t)$. If $v_{sw}(t)$ exceeds the supply voltage $v_{in}(t)$, the BD of $Q_1$ starts to conduct. This yields a shorter turn on delay compared to the previous case of always positive current $i_{L,1}(t)$. Thus, the on-time mismatch $\Delta T_{on}$ is reduced, as shown in Figure 5.7b for $\Delta T_{on,2}$ and $\Delta T_{on,3}$. With more negative $i_L(t)$, the mismatch $\Delta T_{on}$ also shortens, since the steepness of $v_{sw}(t)$ increases due to the faster charging of $C_{DS,1}$ and $C_{DS,2}$. Regarding Figure 5.7a it is worth noting that, the negative current peaks of $i_{L,2}(t)$ and $i_{L,3}(t)$ are linearly approximated. For simplicity, the quadratic behavior of $i_{L,2}(t)$ and $i_{L,3}(t)$ during the charging of $C_{DS,1}$ and $C_{DS,2}$ is neglected in this schematic view. As a consequence of the linear approximation, the valley points of the coil currents occur at different time instances.

Generally, the same switching node behavior can happen at the falling edge of $c(t)$. If $i_L(t)$ is positive, $Q_1$ is turned off and the BD of $Q_2$ starts to conduct during the dead-time $T_p$. Instead, for negative coil current during $T_p$, $C_{DS,1}$ and $C_{DS,2}$ are charged and $Q_1$’s BD starts to conduct, hence $T_{on,sw}$ increases.
Table 5.1: Buck converter parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{in}} )</td>
<td>3.3 V</td>
<td>( L )</td>
<td>3.3 ( \mu )H</td>
</tr>
<tr>
<td>( C )</td>
<td>22 ( \mu )F</td>
<td>( R_p )</td>
<td>105 m( \Omega )</td>
</tr>
<tr>
<td>( R_C )</td>
<td>10 m( \Omega )</td>
<td>( R_l )</td>
<td>8.3 ( \Omega )</td>
</tr>
<tr>
<td>( T_{\text{sw}} )</td>
<td>1 ( \mu )s</td>
<td>( T_p, T_n )</td>
<td>20 ns</td>
</tr>
<tr>
<td>( f_n )</td>
<td>18.8 kHz</td>
<td>( f_{n,d} )</td>
<td>18.5 kHz</td>
</tr>
</tbody>
</table>

5.3.3 On-time perturbation analysis

A parameter which can be used for controller tuning is the natural frequency [40], [47]. For the buck converter model derived in Section 2.2.3, this frequency can be calculated by [72]

\[
f_n = \frac{1}{2\pi} \sqrt{\frac{R_l + R_p}{LC (R_l + R_C)}},
\]

(5.49)

if the exact component values are known.

In the following, a concept for obtaining an estimate of the natural frequency \( f_0 \) by exploiting the on-time mismatch caused by the effect explained before is proposed. For this purpose, the converter is operated under light load conditions with partially negative coil current. This causes the BD of the HS switch \( Q_1 \) to conduct. As a stimulus to the system, the on-time is perturbed with \( \tilde{t}_{\text{on}}(t) \) around its steady state value \( T_{\text{on}} \), yielding the applied on-time \( t_{\text{on}}(t) := T_{\text{on}} + \tilde{t}_{\text{on}}(t) \).

With SSA, the CT small-signal on-time-to-inductor-current TF

\[
G_{i_{\text{on}},i_L}(s) = \frac{\tilde{i}_{\text{on}}(s)}{\tilde{i}_{\text{on}}(s)} = V_{\text{in}} \frac{s + \frac{1}{L(C(R_l + R_C)}}{L s^2 + 2\xi\omega_n s + \omega_n^2 \frac{1}{T_{\text{sw}}}},
\]

(5.50)

with the natural angular frequency

\[
\omega_n = 2\pi f_n,
\]

(5.51)

the damping factor

\[
\xi = \frac{L + C (R_l R_C + R_l R_p + R_C R_p)}{2LC (R_l + R_C) \omega_n},
\]

(5.52)

and the Laplace variable \( s \) can be derived.

As illustrated in Figure 5.8, the peak in magnitude occurs at the so called damped natural frequency \( f_{n,d} \). To be more precise, the amplitude of the inductor current increases the most for an on-time perturbation frequency of \( \omega_{n,d} = 2\pi f_{n,d} \), which can be calculated from (5.50) to be [51]

\[
\omega_{n,d} = \omega_n \sqrt{1 - \xi^2}.
\]

(5.53)
From (5.50), it follows that the peak value of the inductor current depends on the on-time perturbation frequency. The amplitude and phase response of $G_{\text{ton},iL}(s)$, using the converter parameters from Table 5.1, are visualized in Figure 5.8. Note that, the frequency response of $G_{\text{ton},iL}(s)$ is essentially a scaled version of the small-signal on-time-to-inductor-current frequency response reported in Figure 2.14b. The damped natural angular frequency $\omega_{n,d}$ is close to $\omega_n$ for the unloaded converter, because the damping factor $\zeta$ gets smaller with increasing load resistance. The effect of the load on $f_n$ and $f_{n,d}$ is analyzed and reported in Figure 5.9, where $R_l$ is swept from 1 $\Omega$ to 20 $\Omega$. The highest difference between $f_d$ and $f_{n,d}$ is approximately 1 kHz, which is negligibly small when considering controller tuning. Hence, the objective of the SI scheme proposed in this work is to obtain an estimate $\hat{f}_{n,d}$ of $f_{n,d}$ with the approach outlined in the following paragraphs.

In the following, the effect of different on-time perturbation frequencies on the inductor current and subsequently the effect on the on-time mismatch is studied. For that, $T_{\text{on}}$ is superimposed by a 9.5 kHz sinusoidal perturbation $\tilde{t}_{\text{on}}(t)$ with a peak-to-peak amplitude of 100 ns. Figure 5.10 shows the relations between the on-time $t_{\text{on}}(t)$, inductor current $i_L(t)$, switching node voltage $v_{\text{sw}}(t)$ and effective on-time mismatch

$$\Delta t_{\text{on}}(t) := T_p + t_{\text{on}}(t) - t_{\text{on,sw}}(t). \quad (5.54)$$

Here, $t_{\text{on}}(t)$ represents the on-time of the control signal $c(t)$, composed of its steady state value $T_{\text{on}}$ and the small-signal component $\tilde{t}_{\text{on}}(t)$ at the perturbation frequency. Furthermore, $t_{\text{on,sw}}(t)$ denotes the on-time as measured at the switching node. In (5.54), $T_p$ is included in $\Delta t_{\text{on}}(t)$ in order to remove the offset in the on-time mis-
Figure 5.9: Natural frequency $f_n$ and damped natural frequency $f_{n,d}$ as functions of the load resistance $R_l$.

match caused by the dead-time. The on-time modulation causes negative inductor currents, as shown in Figure 5.10b. Consequently, $Q_1$’s BD conducts, which results in an on-time mismatch $\Delta t_{on}(t)$. Also note that, the highest mismatch happens at the lowest average current. The average coil current depends on the frequency of the on-time perturbation. To illustrate this observation, a second case with an on-time perturbation frequency of 19 kHz is shown in Figure 5.11. In this case, the perturbation frequency is close to the damped natural frequency $f_{n,d}$ of the converter and therefore, as shown in Figure 5.11b, a higher peak inductor current can be observed. Thus, a larger on-time mismatch is caused. As can be concluded from Section 5.3.2 and Section 5.3.3, the largest effective on-time mismatch $\Delta t_{on}(t)$ is observed at $f_d$. Since the switching period $T_{sw}$ is kept constant, the natural frequency of the converter can be estimated by superimposing $T_{on}$ with a perturbation $\tilde{t}_{on}(t)$ and measuring the resulting on-time $t_{on,sw}(t)$ of $v_{sw}(t)$. By selecting a linear chirp signal $[101] t_{on,c}(t)$ as the perturbation $\tilde{t}_{on}(t)$, a wide frequency range can be covered and the estimate $\hat{f}_{n,d}$ can be simply derived from the time instant at which the maximum of $\Delta t_{on}(t)$ occurs. To be more precise, for a linear chirp with a start frequency $f_s$, an end frequency $f_e$, and a duration $T_c$, the instantaneous frequency satisfies

$$f_c(t) = \frac{f_e - f_s}{T_c} t + f_s.$$  \hspace{1cm} (5.55)

Thus, the estimate $\hat{f}_{n,d}$ can be found by substituting $t$ in (5.55) with $\arg\max|\Delta t_{on}(t)|$. This is the fundamental principle of the proposed natural frequency estimation approach.
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![Graph of Switching Node Voltage and On-Time](a) Perturbed on-time and resulting switching node waveform. The voltage peaks below 0 V and above 3.3 V are caused by the conduction of the HS BD and LS BD, respectively.

![Graph of Inductor Current and On-Time Mismatch](b) On-time mismatch and inductor current during an on-time perturbation.

**Figure 5.10:** Switching node behavior and on-time mismatch during a sinusoidal on-time perturbation of 9.5 kHz.
(a) Perturbed on-time and resulting switching node waveform. The voltage
peaks below 0 V and above 3.3 V are caused by the conduction of the HS
BD and LS BDs, respectively.

(b) On-time mismatch and inductor current during an on-time perturbation.

Figure 5.11: Switching node behavior and on-time mismatch during a sinu-
soidal on-time perturbation of 19 kHz.
Based on the basic principle discussed in the previous section, an SI concept is introduced in this section. Moreover, a controller tuning approach suitable for a low-complexity implementation is presented. In Figure 5.12, the schematic of the proposed digital SI approach is reported.

5.3.4 Natural frequency estimation concept

During SI, the chirp generator produces the perturbation $t_{on,c,k}$ for the $k$th switching cycle. Since the proposed method requires the on-time mismatch $\Delta t_{on}[k]$, the on-times $t_{on,k}$ and $t_{on,sw,k}$ have to be available in the digital system. As the control command $c_k$ is generated by the system, its on-time $t_{on,k}$ is known. In order to obtain the effective on-time of the switching node voltage, a single bit ADC, e.g., a simple comparator, in combination with a digital counter is sufficient. In more detail, for measuring the on-time of $v_{sw}(t)$, a counter operating at a high rate $\frac{1}{T_{digi}}$, with $T_{digi} \ll T_{sw}$, is employed. This counter is reset upon a rising edge of $v_{sw}(t)$ and stopped upon a falling edge of $v_{sw}(t)$. The transition edges are detected by a comparator. The counter yields the on-time $t_{on,sw,k}$ of $v_{sw}(t)$ with a resolution of $T_d$. Based on the time instant at which the largest mismatch $\max|\Delta t_{on,k}|$ occurs, $f_{n,d}$ is calculated according to (5.55).
5.3.4.2 Controller Tuning

To highlight the benefits of the proposed low-complexity SI method, a controller update scheme, which focuses on simplicity, is presented in this section. For that, the estimated damped natural frequency \( \hat{f}_d \) is used to tune a digital controller with the objective of improving the dynamic performance. A PID voltage mode controller in parallel form with its DT TF given as \([47]\)

\[
C_{\text{low,read}}(z) = K_{p,m} + K_{i,m} \frac{T_{sw}z^{-1}}{1-z^{-1}} + K_{d,m} \frac{1-z^{-1}}{T_{sw}},
\]

(5.56)

with \( K_{p,w}, K_{i,w} \) and \( K_{d,w} \) denoting the proportional, integral and derivative gain, respectively, has been selected. Initially, the controller gains are designed based on the worst case converter parameters, indicated by the subscript \( w \), thus ensuring stability under all operating conditions and parameter variations. In this context, worst case parameters refers to the component set which yields the lowest natural frequency, i.e., a configuration with the highest value for both \( L \) and \( C \). The damped natural frequency \( f_{n,d,w} \) of the converter with worst case parameters is calculated by (5.53). After the estimate \( \hat{f}_{n,d} \) is obtained by the proposed method, the controller is tuned. As a first step, a correction factor

\[
\kappa := \frac{\hat{f}_{n,d}}{f_{n,d,w}}
\]

(5.57)

is introduced. Utilizing this correction factor, it is possible to calculate tuned controller coefficients. In this scheme, which focuses on a low-complexity implementation, it is proposed to simply scale the initial controller coefficients by the correction factor \( \kappa \), yielding the tuned coefficients

\[
K_{p,t} = \kappa K_{p,w},
\]

(5.58a)

\[
K_{i,t} = \kappa K_{i,w},
\]

(5.58b)

\[
K_{d,t} = \kappa K_{d,w}.
\]

(5.58c)

Here, the subscript \( t \) denotes the tuned controller coefficients. Despite its simplicity, the presented tuning method improves the dynamic performance of the controller while maintaining stability, which is affirmed by the experimental results presented in Section 7.3.3.
5.3.5 Simulation results

To demonstrate the proposed chirp stimulus natural frequency estimation approach, a simulation for a converter with the parameters listed in Table 5.1 has been carried out. The duration of the chirp signal has been set to $T_c = 0.5 \text{ ms}$. Moreover, the start and end frequency have been selected as $f_s = 1 \text{ kHz}$ and $f_e = 60 \text{ kHz}$, respectively. The frequency range has been chosen in such a way that it covers $f_{n,d}$. Finally, the peak-to-peak amplitude of $t_{on,c}(t)$ has been set to 50 ns.

The chirp modulated on-time $t_{on}(t)$ of the control signal $c(t)$ and the effective on-time $t_{on,sw}(t)$ at the switching node are reported in Figure 5.13. The largest mismatch $\Delta t_{on}(t)$ can be observed at approximately 150 µs. With (5.55), the estimated damped natural frequency $\hat{f}_{n,d} = 18.7 \text{ kHz}$, which is close to the true value $f_{n,d} = 18.5 \text{ kHz}$, is readily calculated.
IMPLEMENTATION

In this chapter, the prototype system that was used for experimentally validating the proposed control and SI approaches is discussed in detail. The core of the hardware implementation consists of the hysteresis sliding controller for interleaved operation with the presented observer, and the SI schemes. Nevertheless, for a practical realization, further blocks such as ADCs, control interfaces, and drivers for the power stages of the DC-DC converter are essential. The digital design of the control law and the SI methods including all the synthesis and verification steps were carried out by the author of this thesis in System Verilog. As opposed to this, an existing solution was used for the SMPS itself, including the power stages, driver circuitries, and output filter, as well as for the required ADCs.

6.1 SPECIFICATION

As a realistic and challenging scenario to validate the derived concepts, a two-phase synchronous buck converter, employed as a power supply for an automotive microcontroller, was selected. For this application, the input voltage can typically vary in the range from 3 V to 5 V, whereas an accurate output voltage of 1.25 V must be provided by the SMPS. The expected load current ranges from 50 mA to 2 A, whereby abrupt load jumps and drops occur. Finally, a constant switching frequency of 1.56 MHz has to be ensured during steady state.

For the hardware prototype, identical circuit parameters as during simulations were used. For convenience, Table 6.1 summarizes them again. Note that, the same power MOSFETs and inductors were employed in all phases of the multi-phase converter, i.e., \( R_p = R_{p1} = R_{p2} \) and \( L = L_1 = L_2 \). As indicated in the table, mainly due to manufacturing tolerances of the selected components, the inductance and capacitance of the output filter can vary over a wide range. Consequently, one set of controller coefficients cannot ensure stability and a satisfactory dynamic performance over the whole parameter range at the same time. This once again justifies SI followed by controller tuning for this application scenario.

6.2 ANALOG-TO-DIGITAL CONVERTER ARCHITECTURE

For the proposed control scheme with digital current reconstruction, two ADCs are required. The first ADC samples the output voltage
Table 6.1: Buck converter parameters and system specification.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$</td>
<td>3 V-5 V</td>
<td>$V_{ref}$</td>
<td>1.25 V</td>
</tr>
<tr>
<td>$L$</td>
<td>3.3 µH±30 %</td>
<td>$R_p$</td>
<td>220 mΩ</td>
</tr>
<tr>
<td>$C$</td>
<td>20 µF±50 %</td>
<td>$R_C$</td>
<td>10 mΩ</td>
</tr>
<tr>
<td>$I_I$</td>
<td>50 A-2 A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>1.5625 MHz</td>
<td>$f_{digi}$</td>
<td>100 MHz</td>
</tr>
<tr>
<td>$f_{adc,in}$</td>
<td>25 MHz</td>
<td>$f_{adc,out}$</td>
<td>25 MHz</td>
</tr>
<tr>
<td>$V_{q,in}$</td>
<td>20 mV</td>
<td>$V_{q,out}$</td>
<td>5 mV</td>
</tr>
<tr>
<td>$V_{o,in}$</td>
<td>1 V</td>
<td>$V_{o,out}$</td>
<td>0.7 V</td>
</tr>
<tr>
<td>$a_{in}$</td>
<td>6</td>
<td>$a_{out}$</td>
<td>3</td>
</tr>
</tbody>
</table>

$v_{out}(t)$ of the converter. The obtained samples are used by the control law, the SMO, and for SI. The second ADC, as briefly discussed in Chapter 4, is only used by the SMO, in order to increase the robustness of the control scheme against line variations.

In the prototype, an 8-bit tracking topology was used as the architectures of both ADCs. While the output voltage ADC has a quantization step size of $V_{q,out} = 5$ mV and an offset of $V_{o,out} = 0.7$ V, the quantization step size and offset are $V_{q,in} = 20$ mV and $V_{o,in} = 1$ V, respectively, for the input voltage ADC. Furthermore, both ADCs were operated with a sampling frequency of $f_{adc,out} = f_{adc,in} = 25$ MHz. In other words, the output and input voltage samples $v_{out,l}$ and $v_{in,l}$ were obtained with an OS factor of 16 with respect to the nominal switching frequency $f_{sw}$. In Table 6.1, a summary of the ADC specification can be found.

It is well-known that the output of a tracking ADC exhibits a limit cycle oscillation of typically ±1 least significant bit (LSB) in steady state. Because of that, and in order to filter noise, e.g., caused by the switching of the power stage, the output samples of the ADCs are not directly used by the controller and SI implementations outlined in the following sections. Rather, digital first-order LPFs, implemented by the difference equation

$$v_{out,lp,l} = 2^{-a_{out}}v_{out,l} + (1 + 2^{-a_{out}})v_{out,lp,(l-1)}$$

(6.1)
on the digital hardware described in Section 6.4, were used to filter the sampled input and output voltages. For brevity, (6.1) only describes the LPF of the output voltage, since the input voltage LPF is implemented in the same way. Here, $a_{out}$ denotes a design parameter, which determines the cutoff frequency of the LPF. The parameters used during the experiments are reported in Table 6.1. It was chosen in such a way that the limit cycle of the tracking ADC is removed, while simultaneously keeping the influence on the plant dynamics be-
low the switching frequency as low as possible. Note that, (6.1) can be implemented with shift operations instead of multiplications if $\alpha_{\text{out}}$ is integer. This approach was followed for the hardware implementation, in order to reduce the computational complexity.

6.3 Buck Converter

As already mentioned, an existing evaluation printed circuit board (PCB) was used for the synchronous buck converter examined in this work. Each phase of the multi-phase converter, comprising its power stage, output filter, additional driver circuitry, and the aforementioned ADCs, was placed on separate but identical PCBs. In Figure 6.1, the board of one phase is shown. In multi-phase operation, the ADCs of only one phase are used, since the same input voltage is provided to all phases and a common output voltage is generated. In contrast to that, the driver stage of each phase receives a separate control command in order to enable an interleaved operation of the SMPS.
Table 6.2: Sliding mode controller and observer specification

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\omega_{\text{SMC}}$</td>
<td>$2\pi \cdot 55$ kHz</td>
<td>$\zeta_{\text{SMC}}$</td>
<td>0.7</td>
</tr>
<tr>
<td>$\omega_{\text{Tsw}}$</td>
<td>$2\pi \cdot 25$ kHz</td>
<td>$\zeta_{\text{Tsw}}$</td>
<td>1.0</td>
</tr>
<tr>
<td>$\omega_{\Phi}$</td>
<td>$2\pi \cdot 30$ kHz</td>
<td>$\zeta_{\Phi}$</td>
<td>1.0</td>
</tr>
<tr>
<td>$\omega_{\text{SMO}}$</td>
<td>$2\pi \cdot 11$ kHz</td>
<td>$\zeta_{\text{SMO}}$</td>
<td>1.0</td>
</tr>
</tbody>
</table>

6.4 DIGITAL HARDWARE

All the control laws and SI approaches presented in this work were implemented in digital hardware. To that end, an Altera Cyclone IV E EP4CE115 field-programmable gate array (FPGA) with a clock frequency of $f_{\text{digi}} = 100$ MHz was used. Furthermore, the sampling clocks for the ADCs were derived from the digital core clock of the FPGA in order to synchronize the sampling instants with the control logic. The ADC samples are received via the general purpose input/output (GPIO) pins of the FPGA, and the control signals for the power switches are transmitted to the PCBs of the phases in the same fashion. Thanks to the FPGA platform, a fair comparison between different control approaches is easily possible, since all of them can be synthesized on the same hardware. In the next sections, the implementation details and hardware architectures of the control and SI approaches are summarized.

6.5 SLIDING MODE CONTROL AND OBSERVER

The hardware implementation of the sliding mode controller with the current observer was designed for a two-phase converter, i.e., two of the previously discussed evaluation boards were used and connected together. In terms of the target closed-loop performance, the same specifications as during simulations were selected. In Table 6.2, the specification parameters for the controller and observer are summarized. As motivated in Section 3.4, other hysteresis SMC approaches are not able to achieve an interleaved operation for this kind of two-phase topology. Hence, this converter configuration further highlights the advantage of the hysteresis modulation scheme proposed in Chapter 3. Starting from the overall structure of the sliding mode controller reported in Figure 3.3, the hysteresis modulation loop shown in Figure 3.5, and the SMO given by (4.15), some further details have to be considered for a practical implementation on the prototyping hardware.

The requirement that the sliding surfaces and the observer output have to be updated with $f_{\text{digi}}$, i.e., in one clock cycle of the digital core, results in a quite challenging computational schedule. Therefore, sim-
ilar to the already outlined LPF implementation, all multiplications in
the controller and observer were approximated by shift operations.
Another potential advantage of this approach is the possible reduc-
tion of area and power consumption, which is especially important
in an application-specific integrated circuit (ASIC) implementation
of the control algorithm. In order to further optimize the computa-
tional schedule, three different clock rates were used in the design.
These are the clock frequency $f_{\text{dig}}$ of the digital core, the sampling rate $f_{\text{adc}}$
of the ADCs, and the nominal switching frequency $f_{\text{sw}}$, whereby the
latter two were derived from $f_{\text{dig}}$ by means of simple counters.

6.5.1 Sliding surface calculation

As discussed in Chapter 4, the AC components of the inductor cur-
rents are required in order to calculate the sliding surface of each
phase. Therefore, the SMO given by the system of difference equa-
tions (4.15), has to operate with $f_{\text{dig}}$. In contrast to that, the output
voltage samples arrive at a clock rate of $f_{\text{adc}}$ and are then filtered
at the same rate. Hence, it is not necessary to update the common
part of the sliding functions with a higher frequency than $f_{\text{adc}}$. Con-
sequently, $\sigma_{c,l}(x_{c,l})$ is also only updated right after $v_{\text{out,lp,l}}$ has been
calculated, i.e., with a frequency of $f_{\text{adc}}$. The current balancing term is
updated only once per nominal switching period. This is reasonable,
since only the DC components have to be balanced.

6.5.2 Hysteresis width calculation

The length of the $k$th switching period, measured in multiples of
$m = \frac{1}{f_{\text{dig}}}$, is available with one cycle delay. Therefore, $C_{\text{t}_{\text{out}}}(z)$ and
$C_{\Phi}(z)$ are operated at $f_{\text{sw}}$, which means that $h_{n,k}$ is also updated
with this rate. Note that, the update instants of $h_{1,k}$ and $h_{2,k}$ occur not
at the same time. Rather, a difference of $\frac{1}{f_{\text{sw}}}$, i.e., the required delay
for interleaving, is deliberately introduced, to synchronize the update
instants of $h_{1,k}$ and $h_{2,k}$ with the rising edges of $c_{1}$ and $c_{2}$, respectively,
in steady state.

6.5.3 Control command calculation

In order to reduce the required bit width and calculation time, the
sliding sum $\sigma_{n,m}(x_{c,m})$ is actually not directly calculated. Instead,
the switching decision for $c_{n,k}$ is evaluated by comparing the induct-
or current $i_{L_{n,m}}$ to the offset hysteresis limits $(h_{n,k} - \sigma_{c,l}(x_{c,l}))$ and
$-(h_{n,k} - \sigma_{c,l}(x_{c,l}))$. 
The synthesis results of the discussed design for the employed FPGA are reported in Table 6.3. As can be seen, no multipliers were used and the targeted clock frequency can be achieved even for the slow corner.

6.6 SYSTEM IDENTIFICATION

In this section, hardware implementation details of the proposed SI approaches are discussed. The architecture of the R-SALS algorithm and the stimuli generator are covered. In contrast to the sliding mode controller, multipliers were used in the design of the R-SALS estimator, which results in a larger complexity. Nevertheless, as supported by the experimental results presented in Section 7.3.1, the proposed approach requires less operations than state-of-the-art parametric SI approaches. Then, the necessary changes to the SI architecture in order to support the sliding mode controller are outlined. Finally, the implementation of the low-complexity natural frequency estimation approach is also addressed.

6.6.1 Parametric system identification

6.6.1.1 Estimation algorithm

For a practical digital hardware realization, in order to reduce implementation effort and area, a fixed point implementation of the SI algorithm is typically preferred. In addition to their high computational complexity, commonly used estimators, such as ILS [88] or ERLS-DCD [84], require a high dynamic range for their calculations. Thus, they are infeasible if low bit widths are demanded. In contrast to that, the proposed R-SALS algorithm can be implemented with relatively low word lengths, while achieving sufficient estimation accuracy. In the next paragraphs, some details of the hardware architecture, which was used for both the state-space-based SI approach with an FSF controller and the SI method for SMC, are outlined.
For the hardware implementation, instead of calculating the cumulative sum \((5.16)\), the row index \(l\) is directly calculated based on a random number drawn from the discrete uniform distribution \(\mathcal{U}\{1, M - 1\}\). Therefore, Line 7 of Algorithm 1, which would require, e.g., a binary search, can also be omitted. Consequently, it is sufficient to generate a total of \(N\) random numbers, each with \(\log_2(M + 1)\) bit, for the row selection strategy. Therefore, the observation matrix randomization does not increase the computational complexity of the algorithm. Although this may decrease the convergence speed in comparison with the row selection strategy \((5.16)\), it has been shown that this kind of random row selection still performs better than a sequential selection of \(l\) [98]. In order to further reduce the computational complexity, all divisions were approximated by shift operations. Therefore, the hardware implementation of the algorithm only requires \(3P + 2\) multiplications per iteration.

### 6.6.1.2 Perturbation sequence

During the SI phase of the state-space-based approach, the duty cycle \(d_{c,k}\) is superimposed by the perturbation \(d_{p,k}\), which is generated by a 9 bit LFSR operated at \(f_{sw}\). Since the amplitude of \(d_{p,k}\) determines the magnitude of the output voltage and inductor current perturbations, a trade-off between estimation accuracy and acceptable excursion around the nominal value of \(v_{\text{out}}(t)\) has to be made. An amplitude of \(\pm 5\) DPWM steps was selected for \(d_{p,k}\). This choice yields a deviation of approximately \(\pm 6.5\%\) around the nominal output voltage value \(V_{\text{ref}}\), while achieving a satisfactory estimation accuracy. The injection time has been set to 0.330 ms, which corresponds to one LFSR cycle or \(M = 511\) input and output samples. Similar to the amplitude of \(d_{p,k}\), the stimulus injection time constitutes a design parameter. On the one hand, longer injection times typically improve the estimation accuracy. On the other hand, the number of rows of the observation matrix \(H\) is determined by \(M\), hence, more multiplications are required. Finally, a fixed number \(N = 511\) was selected for the number of estimation iterations. With the estimation algorithm running at the digital clock rate \(f_{\text{digit}}\), this results in an calculation time of 5.11 \(\mu\)s, which is negligible in comparison to the stimulus injection time. Note that, the R-SALS algorithm can only start with the estimation after the stimulus injection is finished, since all samples have to be available for the observation matrix randomization.

In the SI method for SMC, as for the state-space-based approach, one full cycle of a 9 bit LFSR was used as the stimuli during the SI phase. The amplitude of \(\hat{d}_{c,k}\) was set to \(V_{\text{ref}}/10\), in order to accomplish an acceptable trade-off between estimation accuracy and output voltage perturbation.

It should be noted that the relatively large perturbation amplitudes and stimulus injection times selected for both SI methods in this
work are not required for the proposed estimator to work in general. Rather, these design parameters have been chosen in order to achieve a high estimation accuracy although a low resolution ADC is employed, which also poses a challenge on other estimation algorithms. For the target application, this is acceptable since relaxed constrains on the output voltage regulation apply during a dedicated SI phase, which directly follows after converter start-up.

### 6.6.2 Synthesis results

The synthesis results of the proposed SI approach on an Altera Cyclone IV E EP4CE115 FPGA are reported in Table 6.4. Here, the R-SALS algorithm was implemented in such a way that a single iteration is finished within one clock cycle. Consequently, the number of multipliers can be further reduced if an increased number of required clock cycles per iteration are acceptable.

### 6.6.3 Low-complexity natural frequency estimation

In contrast to the previous schemes, for the natural frequency estimation, the clock of the FPGA was set to $f_{\text{digi}} = 200$ MHz, resulting in a DPWM resolution of $T_{\text{digi}} = 5$ ns. This choice was made in order to improve the accuracy of the natural frequency estimation approach. A linear chirp signal with a duration of $t_d = 0.5$ ms and a peak-to-peak amplitude of 10 DPWM steps was selected as stimulus $t_{\text{on,c,k}}$. Its frequency range was chosen from $f_s = 1$ kHz to $f_e = 60$ kHz, which ensures that the natural frequencies of the output filter sets listed in Table 7.3 are covered. Finally, the stimulus is superimposed onto a constant on-time of $t_{\text{on}} = 0.5$ µs.
EXPERIMENTAL VALIDATION

In this section, measurement results for the control and SI concepts implemented in hardware are presented. As described in Chapter 6, all digital algorithms were implemented in hardware, while a two-phase and a single-phase buck converter were used as the SMPS.

Firstly, the proposed SMC law with dynamic hysteresis modulation for constant switching frequency and interleaved operation is evaluated. In addition to the hysteresis control loops and the low-complexity SMC implementation, the proposed SMO is used for digital current reconstruction. Then, the state-space-based SI method and the subsequent controller tuning are experimentally verified for an FSF controller. Additionally, the performance of the R-SALS algorithm is investigated. Thirdly, the SMC with SI is applied to a buck converter, and the performance gain achieved by controller tuning is presented. Next, the influence of operating conditions such as the load current and the output filter configuration on the low-complexity natural frequency estimation method are evaluated. Finally, natural frequency based tuning results of a PID controller are reported.

7.1 DEMONSTRATOR SETUP

In Figure 7.1, the schematic of the laboratory setup is shown. Both the input voltage and the load current are emulated by laboratory equipment. The ADCs, power stages, driver circuitries, and output filter are placed on existing evaluation PCBs. As outlined in the previous chapter, each phase is placed on a separate PCB. Therefore, the number of phases is easily altered. The same evaluation platform is used by the company partner Infineon to test controllers for SMPSs. In order to guarantee a fair comparison to other control approaches and competitive products, this setup was left unmodified. To close the control loop with the digital controller, the samples of the input and output voltage ADCs are passed to the FPGA. Conversely, as indicated in the figure, the switching signals are fed back as inputs to the driver stages.

7.2 SLIDING MODE CONTROL AND OBSERVER

In order to verify the proposed digital SMC with an SMO for current reconstruction and evaluate its performance the following experiments are presented in this section:

1. The influence of the dynamic hysteresis modulation loops on
a) the switching frequency and  
b) the phase shift  
are investigated.

2. The transient response of the converter to  
a) a load jump and  
b) a load drop  
is evaluated.

The switching node voltages $v_{sw,1}(t)$ and $v_{sw,2}(t)$ during steady state for a constant hysteresis width, frequency loop only and combined frequency and phase loop are reported in Figure 7.2. The constant hysteresis width $h_{const}$ was calculated such that (3.25) yields the desired switching period length $T_{sw,ref}$. Since the switching period is a function of the converter parameters and operating conditions, the actual switching frequency differs from the desired one, as can be seen in Figure 7.2a. In Figure 7.2b, the switching node voltages with activated frequency control loop are reported. While the desired switching frequency is maintained, no phase shift between $v_{sw,1}(t)$ and $v_{sw,2}(t)$ is obtained. With the additional phase shift enabled, both constant frequency operation and interleaving are obtained, as shown in Figure 7.2c.

The responses to a load jump from 0 A to 2 A and the subsequent load release back to 0 A are reported in Figure 7.3. For comparison, the same load current sequence has also been applied to a configuration with a static hysteresis width and an SR flip-flop SMC implementation, which has been shown to achieve a better dynamic performance than a classical PID controller [25], [50]. As can be seen, the proposed control scheme yields a dynamic performance similar to a constant hysteresis width implementation, while the SR flip-flop implementation exhibits a degraded performance. For the converter under exam,
7.2 SLIDING MODE CONTROL AND OBSERVER

(a) SMC with a static hysteresis width.

(b) SMC with the proposed frequency control loop.
the proposed dynamic hysteresis control scheme reduces the undershoot and overshoots by up to 50 mV, or 20%, in comparison to an SR flip-flop SMC implementation. This is expected, since in the latter one, the control signals $c_1(t)$ and $c_2(t)$ cannot turn on until the synchronization clock event occurs.

7.3 SYSTEM IDENTIFICATION

In this section, measurement results for the different SI approaches proposed in Chapter 5 are presented. In the context of this work, the main objective of SI is to obtain a system model suitable for controller tuning. Therefore, not only the accuracy of the estimation approaches is investigated, but the achievable improvement in dynamic performance is also evaluated. Moreover, if applicable, the obtained results are compared to the state of the art in terms of accuracy, convergence speed, and computational complexity.

7.3.1 State-space-based system identification

For the state-space-based SI method outlined in Section 5.1, the two-phase buck converter prototype introduced in Section 6.1 was used.
Figure 7.3: Comparison of the output voltage response to a load jump from 0 A to 2 A and a load drop from 2 A to 0 A for SMC with a constant hysteresis width, SMC with a dynamic hysteresis width calculated by the proposed frequency and phase control loops, and an SR flip-flop SMC implementation. The reported waveforms are the output voltage $v_{out}$ (50 mV/div with 1.24 mV offset) and the load current $i_l$ (2 A/div); time basis 20 µs/div.

Furthermore, the FSF controller and the identification algorithm were implemented on an FPGA, as described in Section 6.6.1.

To demonstrate the proposed closed-loop SI approach, an initial gain vector $k$ for the FSF controller was chosen such that a wide parameter range of ±50% of the nominal values of $L$ and $C$ is supported. Such a large variation is not uncommon in applications using not only components with large tolerances but also supporting different output filter configurations. For the nominal converter parameters, this results in a closed-loop system response with a bandwidth of $w_n = 2\pi \cdot 15$ kHz and a damping factor of $\zeta = 1$. In Figure 7.4, the perturbed output voltage $v_{out}(t)$ during stimulus injection can be seen. Moreover, a sub-harmonic oscillation in steady state can be observed, caused by the low bandwidth of the initial controller and quantization effects. The duty cycle $d_k$, the output voltage $v_{out,k}$, and the current observer output $\hat{i}_{L,k}$, all as sampled by the FPGA, are reported in Figure 7.5. After stimulus injection, the observation matrix $H$ and measurement matrix $Y$ were processed by the proposed state-space estimation algorithm, which yields the parameter matrix estimate $\hat{\Theta}$.

7.3.1.1 Estimation results

In Figure 7.6a, the frequency response of the duty-cycle-to-output-voltage TF $\hat{G}_{d,v_{out,SS}}(z)$, obtained by $z$-transforming the estimated state-
space model, is reported. Additionally, the estimate $\hat{G}_{d,v_{out},TF}(z)$, directly obtained in the $z$-domain by applying the estimator presented in [72], is shown for comparison. Finally, the frequency response of the converter’s TF $G_{d,v_{out}}(z)$ with the measured component values is also included in Figure 7.6a. As can be seen, similar results can be achieved with both methods, whereby for higher frequencies the state-space approach achieves a better fitting to the reference $G_{d,v_{out}}(z)$. The remaining mismatch between the estimates and the reference, which is not relevant for controller tuning, can be attributed to unavoidable effects such as measurement noise, limited ADC resolution and finite numerical precision.

The frequency response of the duty-cycle-to-inductor-currents TF $\hat{G}_{d,i_{L},SS}(z)$ is depicted in Figure 7.7a. As for the output voltage TF, the proposed state-space-based approach achieves a higher estimation accuracy than a conventional $z$-domain estimation approach. However, a significant deviation of both estimates $\hat{G}_{d,i_{L},TF}(z)$ and $\hat{G}_{d,i_{L},SS}(z)$ from $G_{d,i_{L}}(z)$ can be observed at lower frequencies. In this work, the actual inductor current is not measured but digitally reconstructed. Hence, a mismatch between the real inductor current and the one used by the controller and SI blocks exists [61]. This mismatch is the origin of the estimation error at lower frequencies. Nevertheless, an effective controller tuning is not impeded by this difference, since the system dynamics above the resonant frequency are correctly captured and a higher target closed-loop bandwidth than the resonant frequency is selected. It should also be noted that the TFs $\hat{G}_{d,v_{out},SS}(z)$
7.3 System Identification

Figure 7.5: Input and output samples obtained by the FPGA during stimulus injection.
Figure 7.6: Bode plots of the duty-cycle-to-output-voltage TF $G_{d,v_{out}}(z)$ with the measured component values and its estimates $\hat{G}_{d,v_{out},TF}(z)$, and $\hat{G}_{d,v_{out},SS}(z)$ obtained by the $z$-domain and the state-space estimation approach, respectively, for different output filter configurations.
and $\hat{G}_{i\ell,\text{SS}}(z)$ are not required for the proposed auto-tuning process, which is carried out in state-space, and are only shown as an illustrative example.

### 7.3.1.2 Output filter variation

In order to assess the reliability of the proposed SI approach, different output filter configurations were identified. Exemplarily, the frequency responses of the estimated TFs for a converter configuration with $L_1 = 3.3 \, \mu\text{H}$, $L_2 = 2 \, \mu\text{H}$, and $C = 20 \, \mu\text{F}$ are reported in Figure 7.6b and Figure 7.7b. As can be seen, similar results in terms of estimation accuracy as for the initial output filter configuration, were achieved.

### 7.3.1.3 Convergence speed

The convergence speed of the proposed state-space estimator in comparison with a $z$-domain approach for two different $L$ and $C$ configurations is reported in Figure 7.8a and Figure 7.8b. For this comparison, the cost function (5.9) was evaluated in each iteration step, which is not necessary in the practical estimation process. As references, denoted by BLS, the exact solutions (5.10) of the minimization problems (5.9) are also included in the figures. These solutions have been obtained by calculating $\hat{H}$'s pseudoinverse, a computationally complex operation [88]. Furthermore, the convergence speed and accuracy of the proposed R-SALS algorithm was compared to the ERLS-DCD estimator [84]. This algorithm is often used for parametric SI purposes in the field of SMPSs [35], [71], [73].

A significant improvement in convergence speed, as well as a higher accuracy, was achieved by the state-space estimation compared to the $z$-domain approach. In other words, the proposed approach requires less iterations to obtain an accurate model of the converter. This is further highlighted by Figure 7.9, which shows that the state-space estimation in combination with the R-SALS algorithm requires the fewest number of multiplications. Table 7.1 summarizes the number of multiplications per iteration, as well as the total number of multiplications, for the different approaches. As can be seen, the R-SALS algorithm significantly reduces the number of required multiplications per iteration and consequently, the total number of multiplications in comparison to the state-of-the-art ERLS-DCD algorithm. The value of $J(\hat{\Theta})$ after $N = 511$ iterations is reported in Table 7.2. Although the proposed R-SALS state-space-based approach requires significantly less multiplications than the state-of-the-art ERLS-DCD algorithm, a comparable performance in terms of estimation accuracy is achieved. Again, the analytical solution (5.10) of the LS minimization problem is denoted by BLS, and only included as a reference.
Figure 7.7: Bode plots of the duty-cycle-to-inductor-currents $G_{d_{i_L}} (z)$ with the measured component values and its estimates $\hat{G}_{d_{i_L}, TF} (z)$, and $\hat{G}_{d_{i_L}, SS} (z)$ obtained by the z-domain and the state-space estimation approach, respectively, for different output filter configurations.
Figure 7.8: Cost function $J(\hat{\Theta}^{(n)})$ in dependence of iterations $n$ for the proposed R-SALS algorithm and the ERLS-DCD algorithm applied to state-space and TF estimation for different output filter configurations.
Figure 7.9: Cost function $J(\hat{\Theta}^{[n]})$ in dependence of multiplications per iteration for the proposed R-SALS algorithm and the ERLS-DCD algorithm applied to state-space and TF estimation for different output filter configurations.
### Table 7.1: Comparison of the required number of multiplications.

<table>
<thead>
<tr>
<th>Method</th>
<th>Multiplications</th>
<th>$z$-domain ($P = 8$)</th>
<th>state-space ($P = 6$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R-SALS</td>
<td>$3P + 2$</td>
<td>26</td>
<td>22</td>
</tr>
<tr>
<td>ERLS-DCD [84]</td>
<td>$2P^2 + 3P$</td>
<td>152</td>
<td>90</td>
</tr>
</tbody>
</table>

**Total ($N = 511$)**

<table>
<thead>
<tr>
<th>Method</th>
<th>Multiplications</th>
<th>$z$-domain ($P = 8$)</th>
<th>state-space ($P = 6$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R-SALS</td>
<td>13286</td>
<td>11242</td>
<td></td>
</tr>
<tr>
<td>ERLS-DCD [84]</td>
<td>77672</td>
<td>45990</td>
<td></td>
</tr>
</tbody>
</table>

### Table 7.2: Comparison of the achieved estimation accuracy.

<table>
<thead>
<tr>
<th>Method</th>
<th>$z$-domain</th>
<th>state-space</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLS</td>
<td>$1.50 \times 10^{-2}$</td>
<td>$9.76 \times 10^{-3}$</td>
</tr>
<tr>
<td>R-SALS</td>
<td>$1.78 \times 10^{-2}$</td>
<td>$9.86 \times 10^{-3}$</td>
</tr>
<tr>
<td>ERLS-DCD</td>
<td>$1.52 \times 10^{-2}$</td>
<td>$1.00 \times 10^{-2}$</td>
</tr>
</tbody>
</table>

#### 7.3.1.4 Step size adaption and observation matrix randomization

The effectiveness of the adaptive step size, the step size reduction, and the observation matrix randomization, are highlighted in Figure 7.10. It shows that, the ALS estimator with a fixed step size as described in [86], requires significantly more iterations than the R-SALS estimator in order to converge to the BLS solution. Moreover, as already anticipated, a dynamic step size, calculated according to (5.12), improves the convergence speed, but simultaneously decreases the achievable accuracy. Hence, a step size reduction strategy, e.g., as given by (5.13)-(5.15), is typically required for the SALS and R-SALS estimators. Also, the further improved convergence speed of the R-SALS estimator in comparison to the SALS algorithm is clearly visible. This performance gain is a result of the observation matrix randomization, which causes rows with larger Euclidean norm to be selected with a higher probability. A more detailed analysis of the influence of the step size and the observation matrix randomization on the estimation algorithm can be found in [86] and [87], [98], respectively.

#### 7.3.1.5 Controller tuning

Ultimately, the estimated state-space model was used for automatic tuning of an FSF controller. The target closed-loop bandwidth and damping factor were specified as $w_n = 2\pi \cdot 30$ kHz, and $\zeta = 0.7$, respectively. The required gain vector $k_f$ for fulfilling the specifica-
Figure 7.10: Convergence as a function of iterations for the ALS algorithm, the SALS algorithm without μ reduction, the SALS algorithm, and the R-SALS algorithm for state-space estimation for an output filter configuration with $L_1 = 3.3 \mu H$, $L_2 = 2 \mu H$, and $C = 20 \mu F$.

In this chapter, experimental results of the SI approach for SMC introduced in Section 5.2 are presented. The implementation details of the used prototype system can be found in Section 6.1. As for the state-space-based SI approach presented in the previous section, the R-SALS was used to obtain an estimate of the system dynamics. Since the performance of the R-SALS algorithm in terms of, e.g., estimation accuracy, and convergence speed, was already studied in Section 7.3.1,
(a) Output filter configuration with \( L_1 = L_2 = 3.3 \mu H \) and \( C = 25 \mu F \).

(b) Output filter configuration with \( L_1 = 3.3 \mu H, L_2 = 2 \mu H \) and \( C = 20 \mu F \).

Figure 7.11: Comparison of the output voltage response to a load jump from 0 A to 1 A and a load drop from 1 A to 0 A for two different output filter configurations and with the default and tuned controller coefficients. The reported waveforms are the output voltage \( v_{out} \) (200 mV/div with 1.2 V offset) and the load current \( i_l \) (800 mA/div); time basis 50 µs/div.
7.3.2.1 Estimation results

Since the sliding mode controller does not calculate a duty cycle directly, the relationship between the control signal $v_{c,k}$ and the sampled output voltage $v_{out,k}$ is estimated instead. In Figure 7.12, the bode plot of the estimated TF $\hat{G}_{v_{c},v_{out}}(z)$ is reported. Moreover, the analytical model of $G_{v_{c},v_{out}}(z)$ with the measured components is included as a reference. As can be seen, a good match between $G_{v_{c},v_{out}}(z)$ and its estimate $\hat{G}_{v_{c},v_{out}}(z)$, obtained by the proposed SI method, was achieved. Finally, in order to validate the analytical model of the sliding mode controller derived in Section 5.2, the frequency response obtained by a simulation of the SMPS in the commercial circuit simulator SIMetrix/SIMPLIS is also depicted in Figure 7.12. As the figure shows, the simulation results support the correctness of the analytical model and the accuracy of the estimated TF.

7.3.2.2 Controller tuning

A transient performance comparison for a load jump from 0 A to 1 A followed by a load release for the default controller and tuned controller coefficients is depicted in Figure 7.13. The controller coeffi-
Figure 7.13: Comparison of the output voltage response to a load jump from 0 A to 1 A and a load drop from 1 A to 0 A with the default and tuned controller coefficients. The reported waveforms are the output voltage $v_{\text{out}}$ (100 mV/div with 1 V offset) and the load current $i_l$ (500 mA/div); time basis 20 µs/div.

cients were selected in such a way that a bandwidth of $w_n = 55$ kHz with a damping factor of $\zeta = 0.7$ is obtained. Initially, the controller coefficients were designed for an output filter configuration with $L = 2.2 \mu$H and $C = 10 \mu$F, whereas $L = 3.3 \mu$H and $C = 22 \mu$H were used for the actual converter. As can be seen in the figure, the default controller coefficients result in large under- and overshoots as well long settling times. Utilizing $\hat{G}_{v_{\text{in}},v_{\text{out}}}(z)$ and the approach suggested in Section 5.2.2.1, the controller coefficients were accordingly tuned, such that the set crossover frequency and damping factor requirements were met. For the specific test case, over- and undershoots were reduced by approximately 100 mV, while the settling time was shortened by almost 30 µs.

7.3.3 Low-complexity natural frequency estimation

In order to validate the low-complexity natural frequency estimation approach proposed in Section 5.3, experimental results for the prototype described in Section 6.6.3 were carried out. The five different output filter sets listed in Table 7.3 were used to investigate the applicability of the approach to different converter configurations. Note that, the natural frequencies reported in Table 7.3 were calculated with (5.49) for an unloaded converter.
Table 7.3: Output filter configurations.

<table>
<thead>
<tr>
<th>Set</th>
<th>Inductance $L$</th>
<th>Capacitance $C$</th>
<th>Natural Frequency $f_n$</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.3.1</td>
<td>3.3 $\mu$H</td>
<td>25 $\mu$F</td>
<td>17.5 kHz</td>
</tr>
<tr>
<td>7.3.2</td>
<td>4.7 $\mu$H</td>
<td>32 $\mu$F</td>
<td>13.0 kHz</td>
</tr>
<tr>
<td>7.3.3</td>
<td>2.2 $\mu$H</td>
<td>17 $\mu$F</td>
<td>26.0 kHz</td>
</tr>
<tr>
<td>7.3.4</td>
<td>3.3 $\mu$H</td>
<td>10 $\mu$F</td>
<td>27.9 kHz</td>
</tr>
<tr>
<td>7.3.5</td>
<td>2.2 $\mu$H</td>
<td>10 $\mu$F</td>
<td>33.9 kHz</td>
</tr>
</tbody>
</table>

7.3.3.1 Load current influence

As discussed in Section 5.3.2, the on-time mismatch, and consequently the proposed estimation approach, are influenced by the load current. Ideally, the converter is unloaded, i.e., $I_L \approx 0$, during the injection of the chirp stimulus. In this case, $i_L(t)$ oscillates around 0 A, which ensures that the inductor is negative during a fraction of the switching period $T_{sw}$. The load current depends on the load resistance $R_L$ and the output voltage $V_{out}$, whereby both are assumed to be constant during the SI phase. The influence of $R_L$ on the estimation accuracy was experimentally analyzed for Set 7.3.1 and three different load current levels.

Firstly, the proposed natural frequency estimation approach was carried out for an almost unloaded converter. The effective on-time mismatch $\Delta t_{on,k}$ during the injection of the chirp signal is reported in Figure 7.14a. Here, the estimation error is defined as $\Delta f_{n,d} := |f_{n,d} - \hat{f}_{n,d}|$.

Secondly, a load resistance of $R_L = 8.3 \Omega$ was chosen. For a static duty cycle of $D = 0.5$, this yields an average output current of $I_L \approx 200$ mA. Nevertheless, depending on the perturbation frequency, $i_L(t)$ becomes negative for a fraction of $T_{sw}$. The effective on-time mismatch $\Delta t_{on,k}$ and the estimation error $\Delta f_{n,d}$ for this case are reported in Figure 7.14b. As the figure shows, the estimation error increases in comparison to the unloaded case. Nevertheless, depending on the dynamic performance requirements, the estimate $\hat{f}_{n,d}$ may still be used for controller tuning.

Finally, a 3.7 $\Omega$ load resistor was employed, which leads to an average output current of approximately 450 mA. For this load current, no negative inductor current was observed. Therefore, $\Delta t_{on,k}$ stays almost constant over all frequencies and the proposed approach is not able to estimate the natural frequency correctly.

To conclude, a low load current level is a requirement for the presented low-complexity natural frequency estimation approach. Depending on the target application, the stimulus injection may be carried out during converter start-up, where this requirement is often fulfilled.
Figure 7.14: Comparison of the on-time mismatch $\Delta t_{on,k}$ and the estimated natural frequency $\hat{f}_{n,d}$ during stimulus injection for Set 7.3.1 and three different load resistances.
7.3.3.2 Output filter variation

In this section, measurement results of the natural frequency estimation approach for the output filter sets reported in Table 7.3 are presented. In order to ensure a negative inductor current during a fraction of $T_{sw}$, the converter was operated in unloaded condition. With a frequency range from 1 kHz to 60 kHz, the chirp signal defined in Section 6.6.3 covers the damped natural frequency range of the five different $L$-$C$ combinations. The on-time mismatch and the resulting natural frequency estimate $f_{n,d}$ for Set 7.3.1 are reported in Figure 7.14a, whereas Figure 7.15 reports the results for Set 7.3.2-Set 7.3.5. As the measurement results show, the estimation error lies in the range between 0.15 kHz and 1.26 kHz. This suggests that the proposed low-complexity natural frequency estimation scheme can be used to tune the employed PID controller according to the scheme suggested in Section 5.3.4.2.

7.3.3.3 Controller tuning

After obtaining the estimate $\hat{f}_{n,d}$, it can be used to adapt the PID controller for the employed output filter set. In order to demonstrate the dynamic performance gain of this step, a default controller configuration, which ensures stability for the slowest $L$-$C$ pair was selected. In this context, slow refers to the highest capacitance and inductance value, i.e., set Set 7.3.2, which exhibits the lowest natural frequency. Then, the proposed natural frequency estimation approach was carried out for Set 7.3.2, which is substantially faster than set B. After successful estimation of the natural frequency, as reported in Section 7.3.3.2, the updated controller coefficients were calculated according to (5.57)-(5.58). In order to demonstrate the improvement achieved by the tuning step, a load jump from 0 A to 0.4 A was performed. A comparison between the output voltage responses of a controller configuration with the default and tuned controller coefficients is reported in Figure 7.16. As the figure shows, the tuned controller achieves a reduced undershoot, while stability is maintained. For the system configuration under exam, the undershoot was reduced by 36 mV, or 30%, in comparison with the default controller coefficients.
7.3 System Identification

(a) Mismatch for Set 7.3.2, yielding an estimation error of $\Delta f_{n,d} = 0.15 \text{ kHz}$.

(b) Mismatch for Set 7.3.3, yielding an estimation error of $\Delta f_{n,d} = 1.16 \text{ kHz}$. 

(c) Mismatch for Set 7.3.4, yielding an estimation error of $\Delta f_{n,d} = 1.26 \text{ kHz}$.
Figure 7.15: Comparison of the on-time mismatch $\Delta t_{\text{on},k}$ and the estimated natural frequency $\hat{f}_{n,d}$ during stimulus injection for the unloaded converter and Set 7.3.2-Set 7.3.5.

(d) Mismatch for Set 7.3.5, yielding an estimation error of $\Delta f_{n,d} = 0.68 \text{kHz}$.

Figure 7.16: Comparison of the output voltage response to a load jump from 0 A to 0.4 A for set Set 7.3.4 with the default and tuned controller coefficients. The reported waveforms are the output voltage $v_{\text{out}}$ (50 mV/div with 950 mV offset) and the inductor current $i_L$ (200 mA/div); time basis 20 µs/div.
CONCLUSION AND OUTLOOK

8.1 CONCLUSION

One of the main contributions of this work is a digital constant frequency SMC implementation for multi-phase DC-DC converters. Interleaving as well as a constant switching frequency is achieved by dynamically adjusting the hysteresis widths of the comparators. Small-signal TFs for both the frequency and phase shift control loop were derived for a multi-phase buck converter. The proposed hysteresis modulation can be likewise applied to converters with more than two phases and to a wide range of DC-DC converter topologies. In contrast to state-of-the-art solutions, the proposed concept maintains the required phase shift regardless of the number of active phases and output voltage. Hence, the presented hysteresis modulation scheme can be used, e.g., with two-phase interleaved converters, where other state-of-the-art hysteresis SMC schemes do not maintain an interleaved operation. Furthermore, rather than a direct current measurement, an SMO is employed to digitally reconstruct the inductor currents. Thus, no current sensors and additional ADCs, which would significantly increase the implementation effort in multi-phase converters, are required. Consequently, an efficient, low-complexity, and fully digital controller implementation is possible. Experimental results for a two-phase synchronous buck converter showed that the proposed approach achieves constant frequency and interleaving while not degrading the performance of hysteresis SMC. In comparison to an SR flip-flop implementation of SMC, an improvement of 20% was achieved in terms of over- and undershoots.

Moreover, different SI methods for DC-DC converters were introduced in this thesis. First, a parametric state-space-based SI approach was presented. The proposed approach combines the efficient SALS algorithm with observation matrix randomization. Furthermore, in contrast to state-of-the-art solutions, the SI is carried out in state-space instead of the z-domain. This enables a fast and accurate estimation of the plant with low computational complexity. Subsequently, the estimated model was used to automatically tune an FSF controller, improving both its static and dynamic performance. Experimental results for a two-phase buck converter highlighted the fast convergence speed and accuracy of the proposed SI concept as well as the performance gain of the auto-tuning. In order to adapt the SI scheme for SMC, modifications to the sliding surface definition were proposed. To that end, a control structure enabling a simple stimuli injection
and straightforward controller tuning was introduced. Again, this SI approach utilizes the low-complexity R-SALS for estimating the coefficients of the control to output TF. Consequently, the controller coefficients are automatically tuned by utilizing the estimation result, yielding an improved dynamic performance of the SMPS compared to the initial controller. Reusing the implemented SI estimation algorithm for controller tuning allows for an efficient hardware implementation. The experimental results for a synchronous buck converter emphasized the accuracy and convergence speed of the proposed SI method and the subsequent auto-tuning. The accuracy of the presented estimation algorithm was achieved with less than half the multiplications required for other common estimators. Moreover, an overshoot, undershoot, and settling time reduction by approximately 40% after controller tuning were observed.

Finally, a low-complexity natural frequency estimation approach for SMPSs was proposed. In contrast to parametric SI concepts, costly calculations and high resolution ADCs are not required. Instead, the natural frequency estimation scheme exploits the behavior of the HS MOSFET’s DS capacitance and its BD during dead-times with negative coil currents. Due to its simplicity, the proposed method is well suited for practical on-chip realizations. The theoretical foundations of the method were experimentally verified with a buck converter and different output filter sets. Ultimately, experimental results for a low-complexity automatic controller tuning approach based on the estimated natural frequency were shown. For the presented converter, dynamic performance was improved significantly, i.e., the magnitude of the output voltage transient was reduced by 30% compared to the untuned controller.

8.2 Outlook

A first order SMC with a linear sliding surface definition was chosen for the presented sliding mode controller. However, using higher order sliding modes or a non-linear sliding surface may further improve the dynamic response of the SMPS, while potentially increasing the implementation complexity. Therefore, investigating higher order sliding mode controllers, possible non-linear sliding surface candidates, and their practical implementation would be an interesting topic for further research.

In recent times, machine learning and neural network based approaches have gained a lot of interest in the context of SI. Incorporating these techniques in an on-line controller tuning approach is an open question, which still has to be addressed in the field of SMPSs.

So far, all control and SI algorithms were implemented on an FPGA. This approach enables a fair and simple comparison of the different methods and algorithms. Furthermore, new features can be quickly
implemented and experimentally verified. Nevertheless, for a practical implementation, the control structure and the SI would be typically implemented on a custom chip. This integration has not been exercised within the framework of this thesis and could be investigated in a future work.


